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# CT-CCVAX

Intel® Atom D2000/N2000 Series

COM Express™ Type 10 Module

User's Manual

Version 1.0

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# I. Preface

## 1.1 Disclaimer

All specifications and information in this User's Manual are believed to be accurate and up to date. C&T Solution Inc. does not guarantee that the contents herein are complete, true, accurate or non-misleading. The information in this document is subject to change without notice and does not represent a commitment on the part of C&T Solution Inc.

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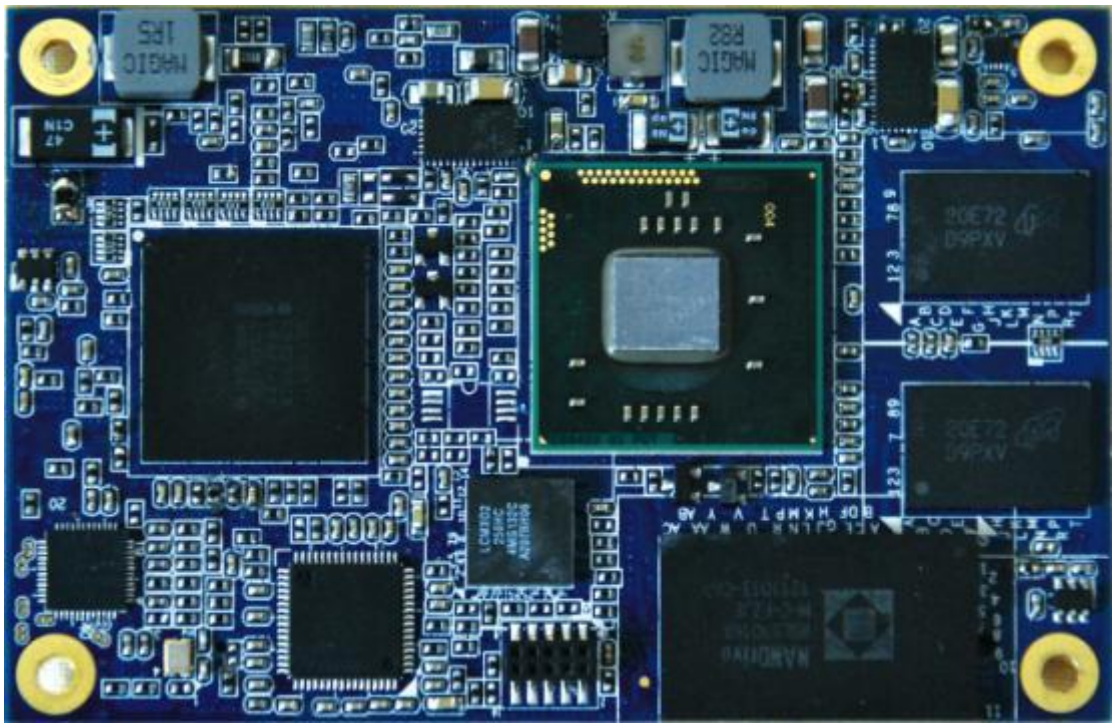
# II. Introduction

## 2.1 Product Description



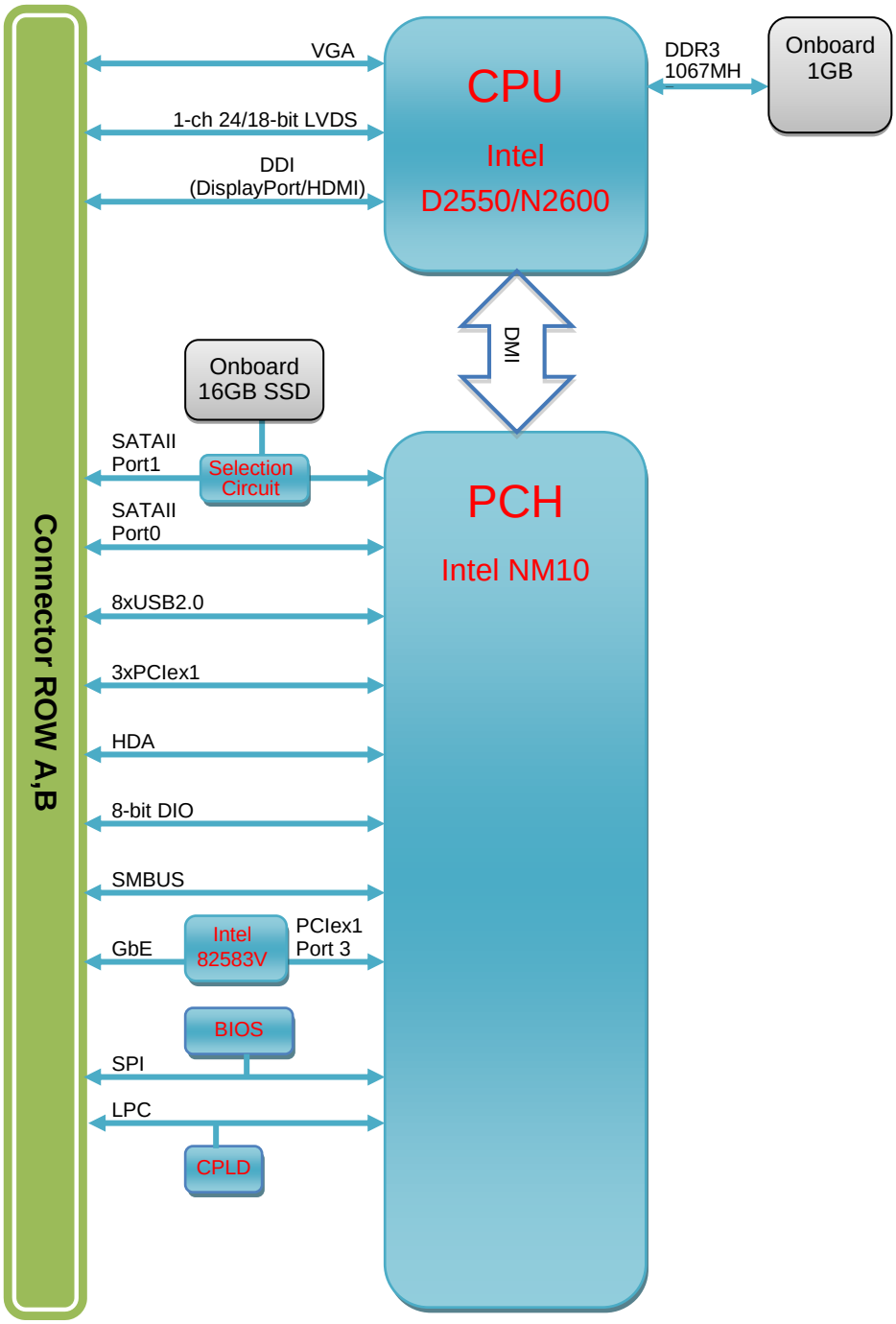
The CT-CCVAX is a new COM (computer-on-module) Express® mini form factor (84x55mm) in embedded computing platforms. It combines the onboard Intel® Atom D2550/N2600 processor with Intel® NM10 Express chipset. The CT-CCVAX is based on the COM Express® specification and features a standardized connector layout that carries a specified set of signals. With the Type 10 pin-out connector, the CT-CCVAX supports DDI/LVDS/VGA, SATA, HD audio, Gigabit Ethernet, PCIe and USB2.0. This system requires a Carrier Board to bring out I/O and power up. The benefit of this standardization pin-out is making the application design more flexible. To accommodate different ODM requirements, the COM Express module with a Carrier Board is the best cost-effective solution and reduces development time.

## 2.2 Specifications

- **CPU**
  - Intel® Atom D2550 processor, 1.86GHz
  - Intel® Atom N2600 processor, 1.6GHz
- **Chipset**
  - Intel® NM10 PCH
- **System Memory**
  - Onboard 1GB DDR3
  - 1066MHz
  - 2GB is optional
- **BIOS**
  - AMI uEFI BIOS
  - 2MB SPI Flash ROM
- **SSD**
  - 16GB SSD onboard
- **Graphics**
  - Dual display
  - Graphic core frequency
    - 640MHz at D2550 processor
    - 400MHz at N2600 processor
  - CRT interface supports up to 1920x1200
  - Single channel of LVDS interface
    - 1-ch 24-bit LVDS supports resolution up to 1440x900 MHz at D2550 processor
    - 1-ch18-bit LVDS supports resolution up to 1366x768 MHz at N2600 processor
  - Two DDI ports supports HDMI / DVI / DisplayPort / eDP
- **Ethernet**
  - Intel® 82583V GbE controller
  - One 10/100/1000 Base-Tx
- **Audio**
  - Integrated in chipset Intel® NM10
- **SATA Interface**
  - One SATA 3Gb/s port
  - Optional second SATA

- **PCIe Lane**
  - Three PCIex1 Lane
- **USB Interface**
  - Eight USB 2.0 ports
- **LPC Interface**
- **SMBus**
- **I2C**
- **8-bit GPIO**
- **Watchdog Timer**
- **H/W Monitor**
- **Power Management**
  - ACPI (Advanced Configuration and Power Interface)
- **Form Factor**
  - Mini size, 84mm x 55mm

## 2.3 Block Diagram



## 2.4 SKU

| Product Number | Processor | PCH | Features |
|---|---|---|---|
| CT-CCVA1 | Intel Atom D2550 | NM10 | Onboard 1GB DDR3, 24-bit LVDS, 3xPCIex1, GbE, 8xUSB2.0, 1xSATA, onboard 16GB SSD |
| CT-CCVA2 | Intel Atom N2600 | NM10 | Onboard 1GB DDR3, 18-bit LVDS, 3xPCIex1, GbE, 8xUSB2.0, 1xSATA, onboard 16GB SSD |

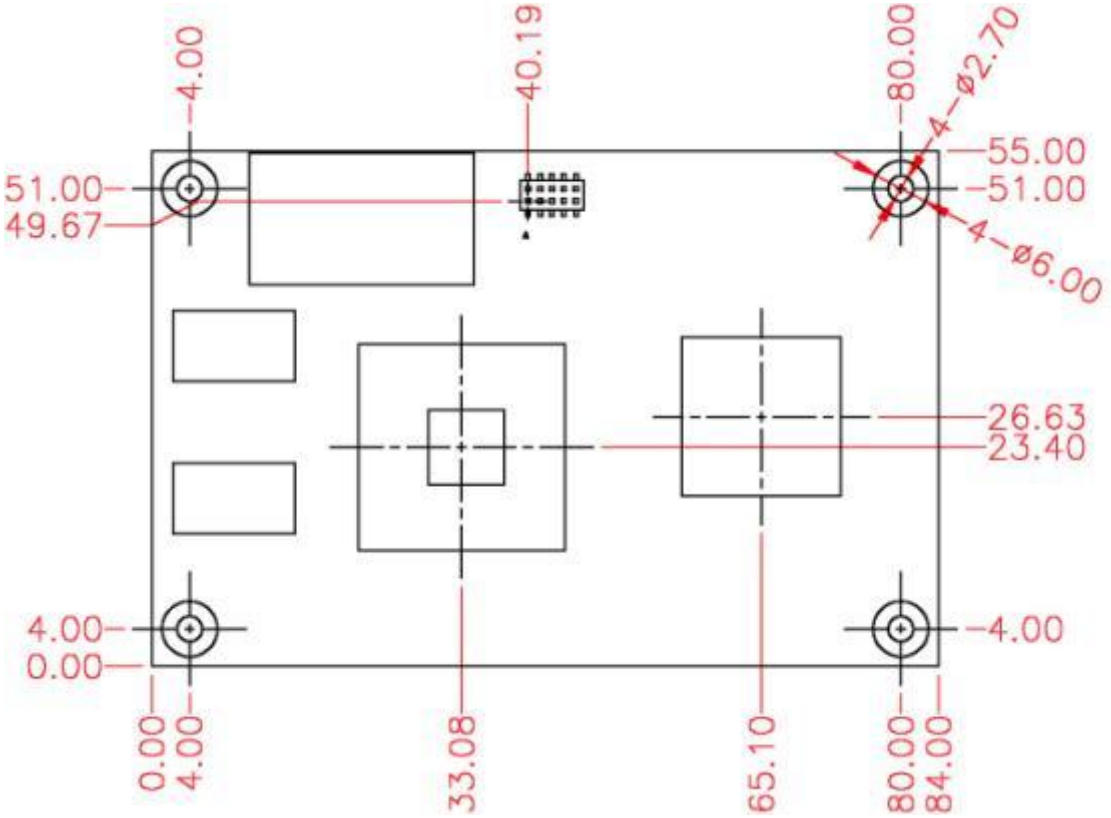
# III. Mechanical Specification

## 3.1 Module Dimensions

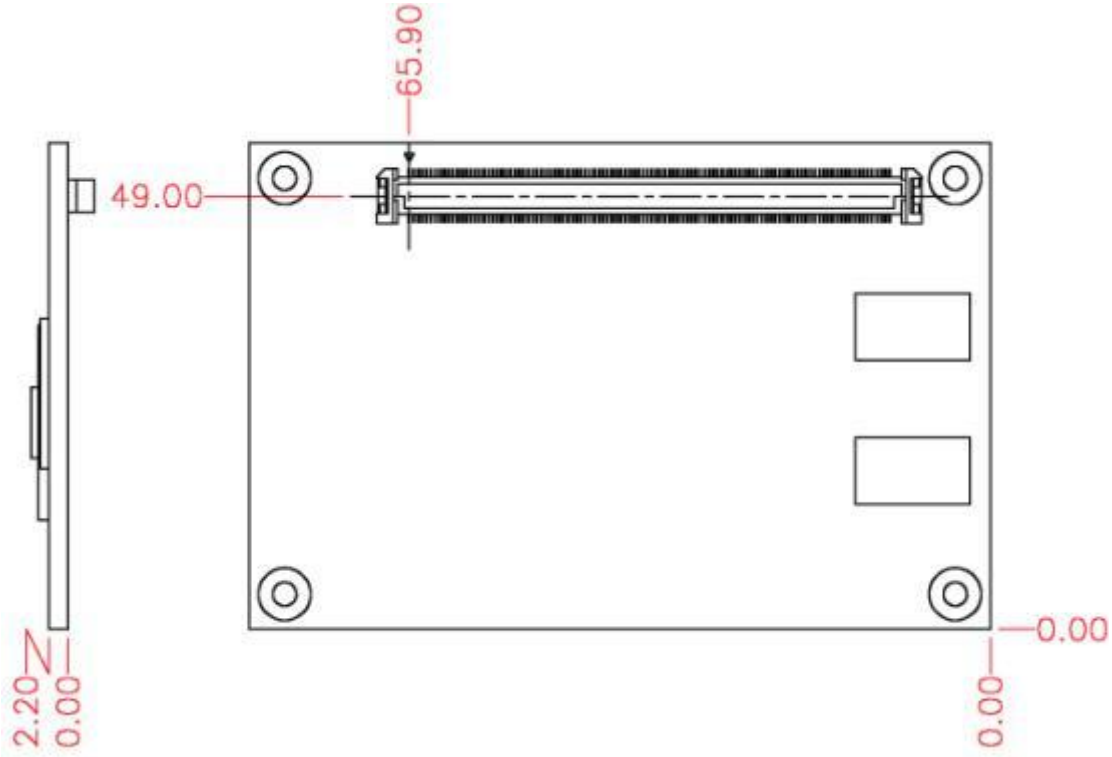
The PCB size of CT-CCVAX is 84mm x 55mm, the standard COM Express mini Module size.

The holes shown in the drawing below is for stacking the module with the Heat Spreader / Heat Sink and the Carrier Board. The mounting holes are 2.7mm, and the 2.5mm hardware shall be used. The position and the dimension of the holes are shown in the unit of millimeters.

**Top View:**



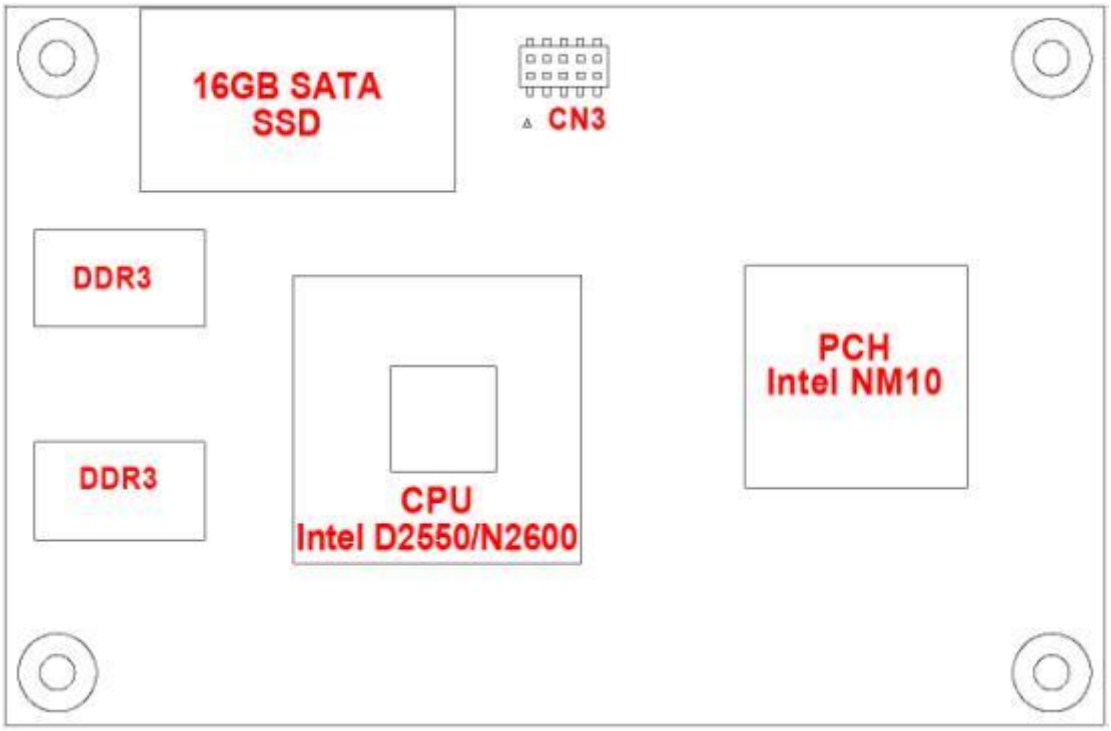
**Side View and Bottom View:**



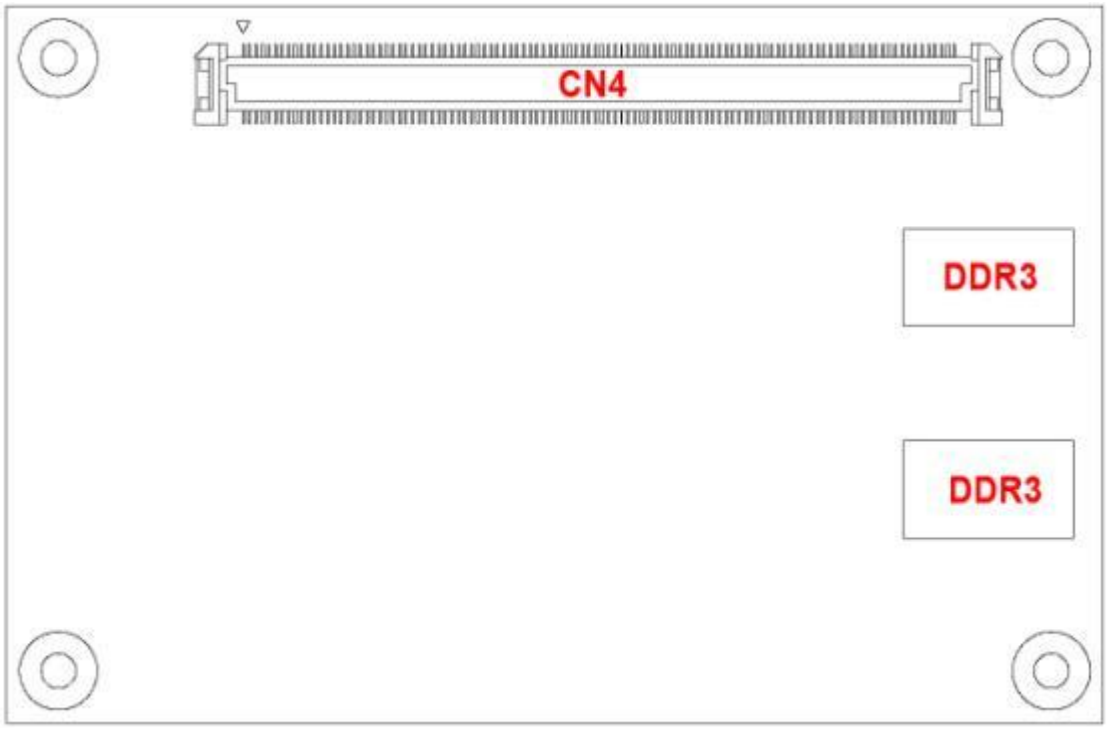

## 3.2 Layout

One 220-pin COM Express connectors are mounted at the bottom side of the PCB.

**Top View:**




**Bottom View:**



# 3.3 Connectors

| Connector | Description |
|---|---|
| CN3 | CPLD JTAGE |
| CN4 | COM™ Express connector Row A, B |

## 3.3.1 LPC Debug Port: CN3

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | 3.3V | 2 | GND |
| 3 | TDO | 4 | GND |
| 5 | TDI | 6 | GND |
| 7 | TMS | 8 | GND |
| 9 | TCK | 10 | GND |

## 3.3.2 COM Express Connectors

The CT-CCVAX is connected to the carrier board via one 220-pin connector, CN4. The connector is break down into two rows. The pin-out is as table below.

| Pin | Row A | Row B |
|---|---|---|
| 1 | GND | GND |
| 2 | GBE0_MDI3- | GBE0_ACT# |
| 3 | GBE0_MDI3+ | LPC_FRAME# |
| 4 | GBE0_LINK100# | LPC_AD0 |
| 5 | GBE0_LINK1000# | LPC_AD1 |
| 6 | GBE0_MDI2- | LPC_AD2 |
| 7 | GBE0_MDI2+ | LPC_AD3 |
| 8 | GBE0_LINK# | LPC_DRQ0# |
| 9 | GBE0_MDI1- | LPC_DRQ1# |
| 10 | GBE0_MDI1+ | LPC_CLK |
| 11 | GND | GND |
| 12 | GBE0_MDI0- | PWRBTN#- |
| 13 | GBE0_MDI0+ | SMB_CK |

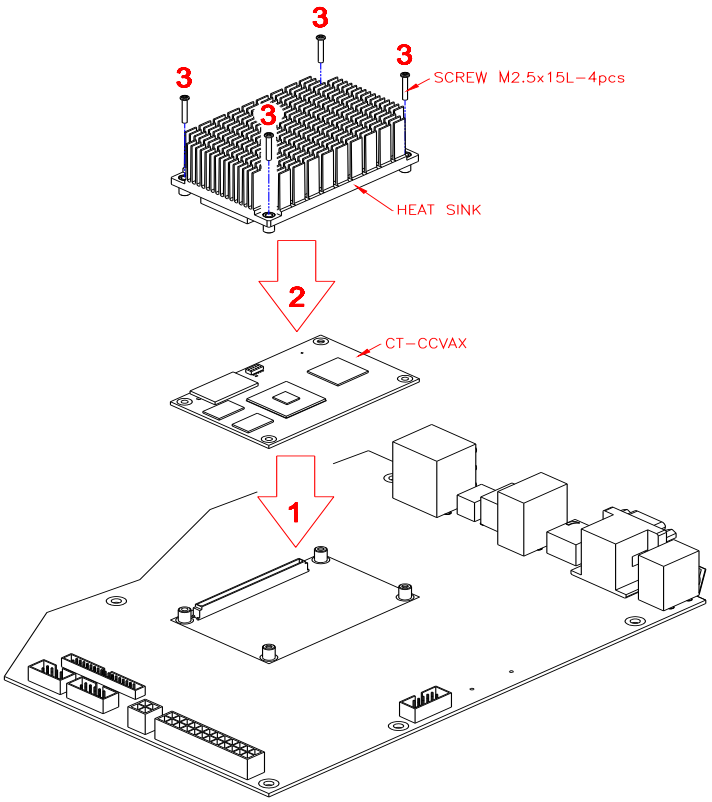
| Pin | Row A | Row B |
|---|---|---|
| 14 | GBE0_CTREF | SMB_DAT |
| 15 | SUS_S3# | SMB_ALERT# |
| 16 | SATA0_TX+ | SATA1_TX+ (Reserved) |
| 17 | SATA0_TX- | SATA1_TX- (Reserved) |
| 18 | SUS_S4# | SUS_STAT# |
| 19 | SATA0_RX+ | SATA1_RX+ (Reserved) |
| 20 | SATA0_RX- | SATA1_RX- (Reserved) |
| 21 | GND | GND |
| 22 | NC | NC |
| 23 | NC | NC |
| 24 | SUS_S5# | PWR_OK |
| 25 | NC | NC |
| 26 | NC | NC |
| 27 | BATLOW# | WDT |
| 28 | (S)ATA_ACT# | AC/HAD_SDIN2 |
| 29 | AC/HDA_SYNC | AC/HAD_SDIN1 |
| 30 | AC/HAD_RST# | AC/HAD_SDIN0 |
| 31 | GND | GND |
| 32 | AC/HDA_BITCLK | SPKR |
| 33 | AC/HAD_SDOUT | I2C_CK |
| 34 | BIOS_DIS0# | I2C_DAT |
| 35 | THRMTRIP# | THRM# |
| 36 | USB6- | USB7- |
| 37 | USB6+ | USB7+ |
| 38 | USB_6_7_OC# | USB_4_5_OC# |
| 39 | USB4- | USB5- |
| 40 | USB4+ | USB5+ |
| 41 | GND | GND |
| 42 | USB2- | USB3- |
| 43 | USB2+ | USB3+ |
| 44 | USB_2_3_OC# | USB_0_1_OC# |
| 45 | USB0- | USB1- |
| 46 | USB0+ | USB1+ |
| 47 | VCC_RTC | EXCD1_PERST# |
| 48 | EXCD0_PERST# | EXCD1_CPPE# |
| 49 | EXCD0_CPPE# | SYS_RESET# |
| 50 | LPC_SERIRQ | CB_RESET# |

| Pin | Row A | Row B |
|---|---|---|
| 51 | GND | GND |
| 52 | CRT_RED | CRT_GREEN |
| 53 | NC | CRT_BLUE |
| 54 | GPI0 | GPO1 |
| 55 | CRT_DDC_CLK | CRT_HSYNC |
| 56 | CRT_DDC_DATA | CRT_VSYNC |
| 57 | GND | GPO2 |
| 58 | NC | NC |
| 59 | NC | NC |
| 60 | GND | GND |
| 61 | PCIE2_TX+ | PCIE2_RX+ |
| 62 | PCIE2_TX- | PCIE2_RX- |
| 63 | GPI1 | GPO3 |
| 64 | PCIE1_TX+ | PCIE1_RX+ |
| 65 | PCIE1_TX- | PCIE1_RX- |
| 66 | GND | WAKE0# |
| 67 | GPI2 | WAKE1# |
| 68 | PCIE0_TX+ | PCIE0_RX+ |
| 69 | PCIE0_TX- | PCIE0_RX- |
| 70 | GND | GND |
| 71 | LVDS_A0+ | DDI0_PAIR0+ |
| 72 | LVDS_A0- | DDI0_PAIR0- |
| 73 | LVDS_A1+ | DDI0_PAIR1+ |
| 74 | LVDS_A1- | DDI0_PAIR1- |
| 75 | LVDS_A2+ | DDI0_PAIR2+ |
| 76 | LVDS_A2- | DDI0_PAIR2- |
| 77 | LVDS_VDD_EN | NC |
| 78 | LVDS_A3+ | NC |
| 79 | LVDS_A3- | LVDS_BKLT_EN |
| 80 | GND | GND |
| 81 | LVDS_A_CK+ | DDI0_PAIR3+ |
| 82 | LVDS_A_CK- | DDI0_PAIR3- |
| 83 | LVDS_I2C_CK | LVDS_BKLT_CTRL |
| 84 | LVDS_I2C_DAT | VCC_5V_SBY |
| 85 | GPI3 | VCC_5V_SBY |
| 86 | NC | VCC_5V_SBY |
| 87 | NC | VCC_5V_SBY |

| Pin | Row A | Row B |
|---|---|---|
| 88 | PCIE_CK_REF0+ | BIOS_DIS1# |
| 89 | PCIE_CK_REF0- | DDI0_HPD |
| 90 | GND | GND |
| 91 | SPI_POWER | NC |
| 92 | SPI_MISO | NC |
| 93 | GPO0 | NC |
| 94 | SPI_CLK | NC |
| 95 | SPI_MOSI | DDI0_DDC_AUX_S |
| 96 | NC | NC |
| 97 | NC | SPI_CS# |
| 98 | NC | DDI0_CTRLCLK_AU |
| 99 | NC | DDI0_CTRLCLK_AU |
| 100 | GND | GND |
| 101 | NC | NC |
| 102 | NC | NC |
| 103 | LID# | SLEEP# |
| 104 | VCC_12V | VCC_12V |
| 105 | VCC_12V | VCC_12V |
| 106 | VCC_12V | VCC_12V |
| 107 | VCC_12V | VCC_12V |
| 108 | VCC_12V | VCC_12V |
| 109 | VCC_12V | VCC_12V |
| 110 | GND | GND |

## 3.4 Thermal Solutions

There are two thermal solutions for the COM Module CT-CCVAX to dissipate the heat. One is by using a heat sink and the other one is by using a heat spreader.

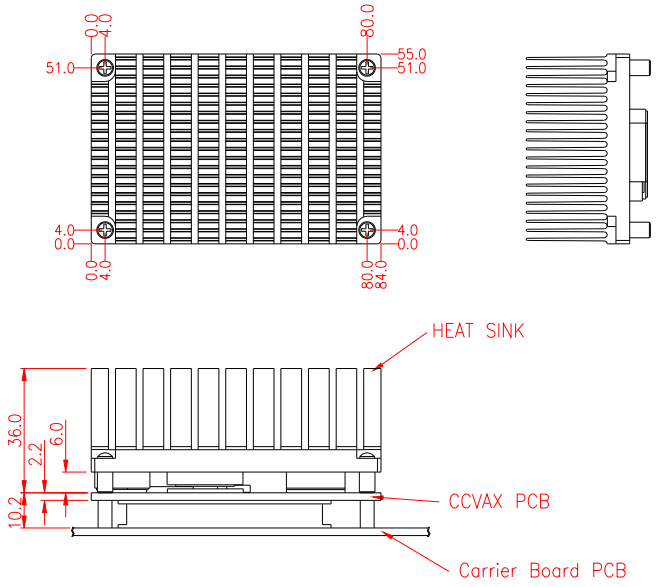



### 3.4.1 Heat Sink

Step 1: Connect the COM Express connectors on the module, CT-CCVAX, to the corresponding COM connectors on the Carrier Board. Make sure the four holes at the corners of CT-CCVAX module align to the corresponding pillars on the Carrier Board.

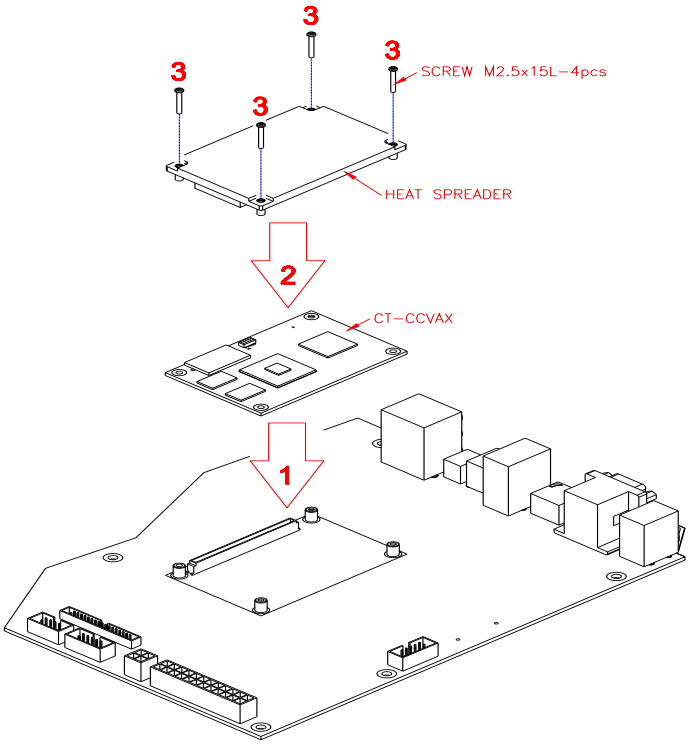
Step2: Place the heat sink on top of the CT-CCVAX module.

Step3: Use four screws (M2.5x15L) to secure the heat sink with the Carrier Board through the corresponding holes on the CT-CCVAX.




### 3.4.2 Heat Spreader

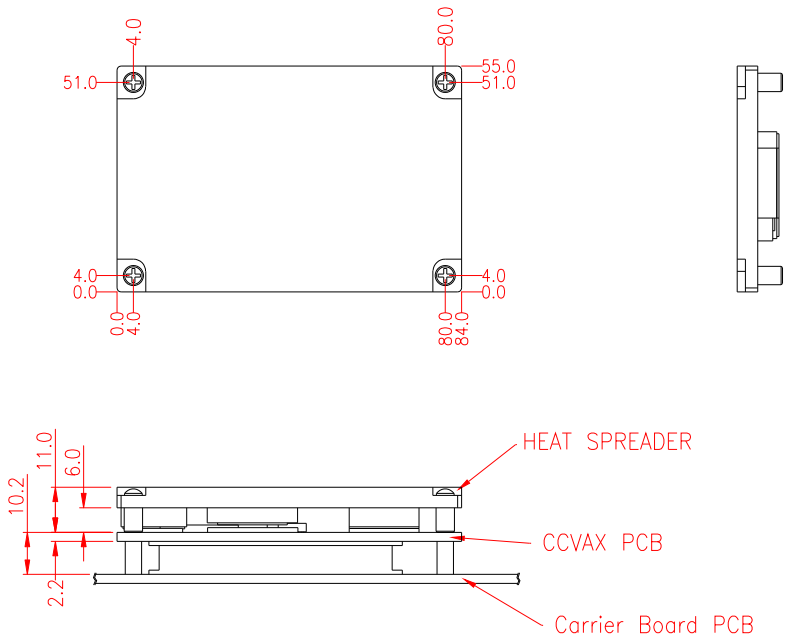
A heat spreader is designed for the CT-CCVAX to dissipate heat. All heat generating components are thermally conducted to the heat spreader in order to avoid hot spots. The assembly of the heat spreader with CT-CCVAX module and the Carrier board is same as the heat sink.



Step 1: Connect the COM Express connectors on the module, CT-CCVAX, to the corresponding COM connectors on the Carrier Board. Make sure the four holes at the corners of CT-CCVAX module align to the corresponding pillars on the Carrier Board.

Step2: Place the heat spreader on top of the CT-CCVAX module.

Step3: Use four screws (M2.5x15L) to secure the heat sink with the Carrier Board through the corresponding holes on the CT-CCVAX.



# IV. Features & Interfaces

## 4.1 Processor

The CT-CCVAX supports Intel® Atom D2550/N2600 processor. This 64-bit and multi-core mobile processor built on 32-nanometer process technology is based on a new micro-architecture. This architecture consists a processor and Platform Controller Hub (PCH) to form a two-chip platform. The processor includes Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

## 4.2 BIOS

The AMI uEFI BIOS, 2MB SPI Flash ROMis used in the CT-CCVAX module.

## 4.3 System Memory

The Integrated Memory Controller (IMC) of the processor supports one 64-bit channel of DDR3 protocols. The channel allows the data transfer rate of 1066MHz. The memory size is 1GB onboard, and 2GB is optional.

## 4.4 Graphics

Intel Atom Processor D2550 and N2600 contain an integrated graphics engine, video decode and a display controller that supports two pipes to LVDS, CRT, HDMI/DVI, DP, eDP. The graphic core frequency is 640 MHz at D2550 and 400 MHz at N2600.

### 4.4.1 Analog Display Port

The Analog Port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated Display Data Channel (DDC) signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT Based monitor with a VGA connector. The Analog Port can directly drive a standard progressive scan analog monitor up to a resolution of 1920x1200 pixels with 32-bit color at 60Hz.

| Signal | I/O | Description |
|---|---|---|
| CRT_RED | O | Red for monitor, analog DAC output, designed to drive a 37.5Ω equivalent load. |
| CRT_GREEN | O | Green for monitor, analog DAC output, designed to drive a 37.5Ω equivalent load. |
| CRT_BLUE | O | Blue for monitor, analog DAC output, designed to drive a 37.5Ω equivalent load. |
| CRT_HSYNC | O | Horizontal sync output to VGA monitor |
| CRT_VSYNC | O | Vertical sync output to VGA monitor |
| CRT_DDC_CLK | I/O | Monitor clock line |
| CRT_DDC_DATA | I/O | Monitor data line |

### 4.4.2 LVDS

The LVDS transmitter channel of D2550 consists of 4 data pairs and a clock pair; N2600 consists of 3 data pairs and a clock pair. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals. The maximum resolution is 1440x900 at D2550 CPU and 1366x768 at N2600 CPU.

| Signal | I/O | Description |
|---|---|---|
| LVDS_A[3:0]+ | O | Differential data output – positive<br>LVDS_A3+ support at D2550 only |
| LVDS_A[3:0]- | O | Differential data output – negative<br>LVDS_A3- support at D2550 only |
| LVDS_A_CLK+ | O | Differential clock output - positive |
| LVDS_A_CLK- | O | Differential clock output - negative |
| LVDS_VDD_EN | O | LVDS panel power enable |
| LVDS_BKLT_EN | O | Panel backlight enable control |
| LVDS_BKLT_CTR | O | Panel backlight brightness control |
| LVDS_I2C_CK | I/O | LVDS flat panel I2C clock for EDID read and control. |
| LVDS_I2C_DATA | I/O | LVDS flat panel I2C data for EDID read and control. |

### 4.4.3 Digital Display Interfaces (DDI)

The Intel Atom Processor D2550 and N2600 can drive HDMI, DVI, eDP and Display Port natively. Its two display ports can support up to two different images on two different display devices.

| Signal | I/O | Description |
|---|---|---|
| DDI0_PAIR[0:3]+<br>DDI0_PAIR[0:3]- | O | DDI0 Pair[0:3] differential pairs |
| DDI0_DDC_AUX_SEL | I | Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CTRLCLK and CTRLDATA signals. |
| DDI0_CTRLCLK_AUX+ | I/O | DP AUX+ function if DDI0_DDC_AUX_SEL is no connect |
| | I/O | HDMI/DVI I2C CTRLCLK if DDI0_DDC_AUX_SEL is pulled high |
| DDI0_CTRLDATA_AUX- | I/O | DP AUX- function if DDI0_DDC_AUX_SEL is no connect |
| | I/O | HDMI/DVI I2C CTRLDATA if DDI0_DDC_AUX_SEL is pulled high |
| DDI0_HPD | I | DDI Hot-Plug Detect |

| | Signal | Pin | eDP/DP | HDMI/DVI |
|---|---|---|---|---|
| DDI0 | DDI0_PAIR0+ | B71 | LANE0+ | TMDS_DATA2+ |
| | DDI0_PAIR0- | B72 | LANE0- | TMDS_DATA2- |
| | DDI0_PAIR1+ | B73 | LANE1+ | TMDS_DATA1+ |
| | DDI0_PAIR1- | B74 | LANE1- | TMDS_DATA1- |
| | DDI0_PAIR2+ | B75 | LANE2+ | TMDS_DATA0+ |
| | DDI0_PAIR2- | B76 | LANE2- | TMDS_DATA0- |
| | DDI0_PAIR3+ | B81 | LANE3+ | TMDS_CLK+ |
| | DDI0_PAIR3- | B82 | LANE3- | TMDS_CLK- |
| | DDI0_CTRLCLK_AUX+ | B98 | AUX+ | SCL |
| | DDI0_CTRLDATA_AUX- | B99 | AUX- | SDA |
| | DDI0_DDC_AUX_SEL | B95 | CONFIG1 (pull down to GND) | Pull up to 5V |
| | DDI0_HPD (3.3V active high) | B89 | | |

#### 4.4.3.1 High Definition Multimedia Interface (HDMI)

The HDMI is provided for transmitting uncompressed digital audio and video signals to television sets, projectors and other video displays.

#### 4.4.3.2 Digital Video Interface (DVI)

The PCH digital ports can be configured to drive DVI-D. DVI uses TMDS for

transmitting data from the transmitter to the receiver, which is similar to the HDMI protocol but the audio and CEC. When a system has support for DVI-I port, then either VGA or the DVI-D through a single DVI-I connector can be driven but not both simultaneously.

The HDMI or DVI supports the resolution up to 1920x1200 at 60Hz.

| HDMI Signal | I/O | Description |
|---|---|---|
| TMDS_CLK+<br>TMDS_CLK- | O | HDMI/DVI TMDS Clock differential pair |
| TMDS_DATA[0:2]+<br>TMDS_DATA[0:2]- | O | HDMI/DVI TMDS lanes 0, 1 and 2 differential pairs |
| SCLK | I/O | HDMI/DVI I2C control clock |
| SDA | I/O | HDMI/DVI I2C control data |

#### 4.4.3.3 **Display Port (DP)**

The Display Port is a digital communication interface that utilized differential signaling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. The Display Port supports the resolution up to 2560x1600 at D2550 CPU and 1600x1200 at N2600 CPU.

#### 4.4.3.4 **Embedded DisplayPort (eDP)**

Embedded DisplayPort (eDP) is an embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. The resolution is up to 1920x1080 at D2550 CPU and 1366x768 at N2600 CPU.

| DP Signal | I/O | Description |
|---|---|---|
| LANE[0:3]+<br>LANE[0:3]- | O | Uni-directional main link for the transport of isochronous streams and secondary-data packets |
| AUX+<br>AUX- | I/O | Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access |

## 4.5 Chipset

The Platform Controller Hub (PCH) used on CT-CCVAX is Intel NM10. The PCH provides extensive I/O support with one COM™ Express connector.

## 4.6 USB

### 4.6.1 USB 2.0

The two EHCI Controllers of Intel® NM10 offer eight USB2.0 ports. Each USB2.0 port supports USB 1.1 and 2.0 compliant devices.

| Signal | I/O | Description |
|---|---|---|
| USB[0:7]+<br>USB[0:7]- | I/O | USB differential pairs, channels 0 through 7 |
| USB_0_1_OC# | I | USB over-current sense, USB 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. |
| USB_2_3_OC# | I | USB over-current sense, USB 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. |
| USB_4_5_OC# | I | USB over-current sense, USB 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. |
| USB_6_7_OC# | I | USB over-current sense, USB 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. |

## 4.7 SATA

The PCH NM10 provides two Serial ATA (SATA) ports. The Port 0 and 1 support SATA 3.0 Gb/s device transfers. This interface may be used for Serial Attached SCSI (SAS).

| Signal | I/O | Description |
|---|---|---|
| SATA0_TX+<br>SATA0_TX- | O | Serial ATA 0 transmit differential pair |
| SATA0_RX+<br>SATA0_RX- | I | Serial ATA 0 receive differential pair |
| SATA1_TX+<br>SATA1_TX- | O | Serial ATA 1 transmit differential pair (reserved) |
| SATA1_RX+<br>SATA1_RX- | I | Serial ATA 1 receives differential pair (reserved) |
| (S)ATA_ACT# | OC | ATA (parallel and serial) activity indicator, active low |

The SATA Port 0 of CT-CCVAX can be used for general SATA devices. The SATA Port 1 of CT-CCVAX has been used for onboard 16GB SSD. Also, this interface has been reserved on the COM Express connector Row B. When the onboard SSD of CT-CCVAX is not applied, the interface on the COM Express connector could be used for general SATA devices.

## 4.8 PCI Express

### 4.8.1 PCI Express x1

There are four one-lane PCI Express ports available in the PCH NM10. The ports are compliant to the PCI Express 1.0 specification running at 2.5 Gb/s. Only three PCIe x1 Ports, 0~2, are left on the CT-CCVAX COM™ Express connector since Port 3 is occupied by GbE.

| Signal | I/O | Description |
|---|---|---|
| PCIE[0:2]_TX+<br>PCIE[0:2]_TX- | O | PCI Express Differential transmit Pairs 0 through 2 |
| PCIE[0:2]_RX+<br>PCIE[0:2]_RX- | I | PCI Express Differential receive Pairs 0 through 2 |
| PCIE_CK_REF0+<br>PCIE_CK_REF0- | O | Reference clock output for all PCI Express and PCI Express Graphics lanes |

## 4.9 High Definition Audio

The High Definition Audio (HDA) controller is integrated with PCH NM10. It communicates with the external codec(s) over the Intel® High Definition Audio serial link. The controller consists of a set of DMA engines that are used to

move samples of digitally encoded data between system memory and an external codec(s). The PCH implements a single Serial Data Output signal (HDA_SDOUT) that is connected to all external codecs. Three Serial Digital Input signals (HDA_SDIN[2:0]) provided by the PCH support up to three codecs.

| Signal | I/O | Description |
|---|---|---|
| AC/HDA_RST# | O | Reset output to CODEC, active low |
| AC/HDA_SYNC | O | Sample-synchronization signal to the CODEC(s) |
| AC/HDA_BITCLK | O | Serial data clock generated by the external CODEC(s) |
| AC/HDA_SDOUT | O | Serial TDM data output to the CODEC |
| AC/HDA_SDIN[2:0] | I/O | Serial TDM data input from up to 3 CODECs |

## 4.10 Ethernet

The Intel® 82583V, a fully-integrated Gigabit Ethernet Media Access Control (MAC) provides 10/100/1000Mb/s Ethernet interface. The Intel® 82583V is connected to Port 2 of the PCIe x1 in the PCH. Gigabit transformer has to be designed on the Carrier Board.

The integrated GbE controller contains power management registers for PCIE, so it supports the Advanced Configuration and Power Interface (ACPI) specification. This enables the network-related activity (using an internal host wake signal) to wake up the host.

| Signal | I/O | Description |
|---|---|---|
| GBE0_MDI[0:3]+<br>GBE0_MDI[0:3]- | I/O | Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100 and 10 Mbit/sec modes. Some pairs are unused in some modes, per the following:<br>1000BASE-T / 100BASE-TX / 10BASE-T<br>MDI[0]+/- / B1_DA+/- / TX+/- / TX+/-<br>MDI[1]+/- / B1_DB+/- / RX+/- / RX+/-<br>MDI[2]+/- / B1_DC+/-<br>MDI[3]+/- / B1_DD+/- |
| GBE0_ACT# | OD | Gigabit Ethernet Controller 0 activity indicator, active low |
| GBE0_LINK# | OD | Gigabit Ethernet Controller 0 link indicator, active low |
| GBE0_LINK100# | OD | Gigabit Ethernet Controller 0 100 Mbit/sec link indicator, active low |

| Signal | I/O | Description |
|---|---|---|
| GBE0_LINK1000# | OD | Gigabit Ethernet Controller 0 1000 Mbit/sec link indicator, active low |
| GBE0_CTREF | REF | Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is 3.3V. |

## 4.11 LPC

The LPC interface provides legacy I/O support on a Carrier Board via a Super I/O and system management devices.

| Signal | I/O | Description |
|---|---|---|
| LPC_AD[3:0] | I/O | LPC multiplexed address, command and data |
| LPC_FRAME# | O | LPC frame indicates the start of an LPC cycle |
| LPC_DRQ[0:1]# | I | LPC serial DMA request input |
| LPC_SERIRQ | I/O | LPC serial interrupt |
| LPC_CLK | O | LPC clock output – 33MHz nominal |

## 4.12 SPI

The Serial Peripheral Interface (SPI) is a 4-pin interface that supports SPI-compatible flash devices. The SPI flash device can be up to 16MB (128Mb). The SPI bus is clocked at either 20MHz, 25MHz, 33MHz or 50 MHz. SPI devices selected should support one of these frequencies.

| Signal | I/O | Description |
|---|---|---|
| SPI_CS# | O | Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1 |
| SPC_MISO | I | Data in to Module from Carrier SPI |
| SPI_MISI | O | Data out from Module to Carrier SPI |
| SPI_CLK | O | Clock from Module to Carrier SPI |
| SPI_POWER | O | Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100ma of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board. |

## 4.13 SMBus

The SMBus port is specified for system management functions. It is used on the Module to manage system function such as reading the DRAM SPD EEPROM and setting clock synthesizer parameters. If the SMBus is used on the baseboard, then great care must be taken that no conflicts with the on-Module SMBus devices occur. It may be useful for implementation on the Carrier Board of standards such as Smart Battery. The maximum capacitance on the Carrier Board shall not exceed 100pF.

| Signal | I/O | Description |
|---|---|---|
| SMB_CK | I/OD | System Management Bus bidirectional clock line |
| SMB_DAT | I/OD | System Management Bus bidirectional data line |
| SMB_ALERT# | I | System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. |

## 4.14 ExpressCard

ExpressCard is a small form factor expansion card that uses PCI Express or USB as the interface. It is similar in concept and scope to CardBus. The CT-CCVAX supports two Express Card interface.

| Signal | I/O | Description |
|---|---|---|
| EXCD[0:1]_CPPE# | I | PCI ExpressCard: PCI Express capable card request, active low, one per card |
| EXCD[0:1]_PERST# | O | PCI ExpressCard: reset, active low, one per card |

## 4.15 General Purpose Input Output

GPI and GPO pins may be implemented as GPIO (Module specific). GPI and GPO pins may be implemented as SDIO.

| Signal | I/O | Description |
|---|---|---|
| GPO[0:3] | O | General purpose output pins. Upon a hardware reset, these outputs should be low |
| GPI[0:3] | I | General purpose input pins. Pulled high internally on the Module. |

### 4.15.1 GPIO Configuration

Output Pin default setting is HIGH.

| Pin # | GPIO# | Default Configuration |
|---|---|---|
| B63 | GPIO7 | **GPO3** |
| B57 | GPIO6 | **GPO2** |
| B54 | GPIO5 | **GPO1** |
| A93 | GPIO4 | **GPO0** |
| A85 | GPIO3 | **GPI3** |
| A67 | GPIO2 | **GPI2** |
| A63 | GPIO1 | **GPI1** |
| A54 | GPIO0 | **GPI0** |

The GPIO function, provided by Intel Tiger Point NM10, can be accessed through GPIO Base Address Register (GPIOBASE). The configuration on CT-CCVAX is described as below.

| Register | Address |
|---|---|
| GPIOBASE Base Address | 0x500 |

The general I/O read/write function is used to access and configure the NM10. Through the I/O read or write command, the current status of GPIO can configure each pin to input or output.

### 4.15.2 Registers Description

#### 4.15.2.1 **GPIO Use Select Register 1 (Offset GPIOBASE+0x00)**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | GPIO3 | GPIO2 | GPIO1 | GPIO0 | | |

**GPIO Use Select Register 2 (Offset GPIOBASE+0x30)**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| GPIO7 | GPIO6 | | | | GPIO5 | GPIO4 | |

Bit X = 0 means Native Function

Bit X = 1 means GPIO Function

#### 4.15.2.2 GPIO Input/Output Select Register 1 (Offset GPIOBASE+0x04)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | GPIO3 | GPIO2 | GPIO1 | GPIO0 | | |

**GPIO Input/Output Select Register 2 (Offset GPIOBASE+0x34)**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| GPIO7 | GPIO6 | | | | GPIO5 | GPIO4 | |

Bit X = 0 means Output Pin

Bit X = 1 means Input Pin

#### 4.15.2.3 GPIO Level for Input or Output Register 1 (Offset GPIOBASE+0x0C)

If Pin X is configured as output, the output value (0 or 1) could be selected by user.

If it is programmed as an input, this register reflects the state of the input signal.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | GPIO3 | GPIO2 | GPIO1 | GPIO0 | | |

**GPIO Level for Input or Output Register 1 (Offset GPIOBASE+0x38)**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| GPIO7 | GPIO6 | | | | GPIO5 | GPIO4 | |

#### 4.15.2.4 GPIO Signal Invert Register (Offset 0x2C)

It will invert the polarity of the Input Port register data.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | GPIO3 | GPIO2 | GPIO1 | GPIO0 | | |

Bit X = 0 means Polarity is retained

Bit X = 1 means Polarity is inverted

[Note] The GPIO4~GPIO7 can't be set to inverted.

#### 4.15.2.5 **PSUEDO CODE**

Example 1 Change GPIO2 from output to input

```
Step1: ByteData = ReadIOByte(0x504)      //Read current setting from
                                          configuration register
Step2: ByteData = ByteData | Bit 4        //Set Bit4 1. It means input
Step3: WriteIOByte(0x504, ByteData)      //Write back to configuration register
```

Example2 Set GPIO3 to output LOW

```
Step1: ByteData = ReadIOByte(0x50C)      //Read current setting from Output
                                          Port register
Step2: ByteData =ByteData & 0xDF         //Set Bit5 0. It means output low
Step3: WriteIOByte(0x50C, ByteData)       //Write back to Output Port
Register
```

## 4.16 Power and System Management Signals

| Signal | I/O | Description |
|---|---|---|
| SUS_S3# | O | Indicates system is suspended to RAM state. Active low output. |
| SUS_S4# | O | Indicates system is suspended to Disk state. Active low output. |
| SUS_S5# | O | Indicates system is in Soft Off state. |
| SUS_STAT# | O | Indicates imminent suspend operation. |
| PWRBTN# | I | Power button to bring system out of S5 (soft off), active on rising edge. |
| PWR_OK | I | Power OK from main power supply |
| BATLOW# | I | Indicates that external battery is low. |
| SYS_RESET# | I | Reset button input. Active low input. |
| CB_RESET# | O | Carrier Board Reset. Active low input. |
| WAKE0# | I | PCI Express wake up signal. |
| WAKE1# | I | General purpose wake up signal. |
| VCC_RTC | I | RTC External Battery |
| LID# | I | LID switch |
| SLEEP# | I | Sleep Button |
| FAN_PWMOUT | O | FAN PWM out |
| FAN_TACHIN | I | Fan Tacho in |

## 4.17 Thermal Management Signals

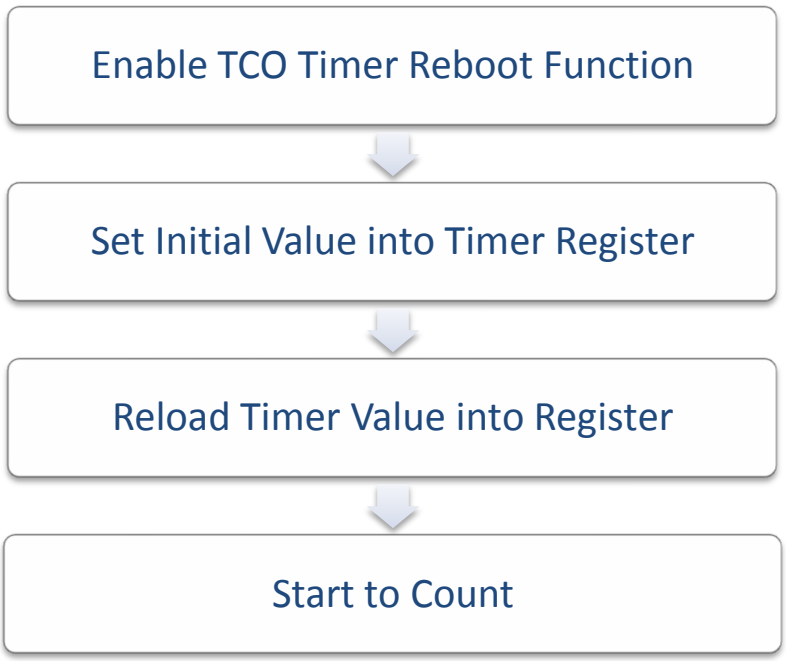
| Signal | I/O | Description |
|---|---|---|
| THRMTRIP# | O | Active low output indicating that the CPU has entered thermal shutdown. |
| THRM# | I | Input from off-module temp sensor indicating and over-temp situation. |

## 4.18 Miscellaneous Signals

| Signal | I/O | Description |
|---|---|---|
| I2C_CK | O | General purpose I2C port clock output |
| I2C_DAT | I/O | General purpose I2C port data I/O lin |
| WDT | O | Indicator for Watchdog Timeout |
| SPKR | O | Output for audio enunciator-the “speaker” in PC-AT systems |
| BIOS_DIS0#<br>BIOS_DIS1# | I | Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to the table below for strapping option of BIOS disable signals. |

| BIOS_DIS1# | BIOS_DIS0# | Chipset SPI CS1# Destination | Chipset SPI CS0# Destination | Carrier SPI_CS# | SPI Descriptor | BIOS Entry | Ref Line |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Module | Module | High | Module | SPI0/SPI1 | 0 |
| 1 | 0 | Module | Module | High | Module | Carrier FWH | 1 |
| 0 | 1 | Module | Carrier | SPI0 | Carrier | SPI0/SPI1 | 2 |
| 0 | 0 | Carrier | Module | SPI1 | Module | SPI1/SPI1 | 3 |

# 4.19 Watchdog Timer




## 4.19.1 Board Design

The WDT (Watchdog Timer) is implemented by using TCO function in NM10.

| Register | Address |
|---|---|
| TCO I/O Base (TCOBASE) | 0x460 |
| RCBA Memory Base (RCBA) | 0xFED1C000 |

Notes:

1. TCO (Total Cost of Ownership)
2. RCBA (Root Complex Base Address)

## 4.19.2 PSUEDO CODE

***Step1*** *Enable TCO Timer Reboot Function*

**Target: Clear RCBA+3410h Bit 5 to 0**

```
Step1: DWordData = ReadMemoryDword(0xFED1F410)     //0xFED1C000+0x3410
Step2: DWordData = DWordData & 0xFFFFFFDF          //Clear DWordData Bit
                                                     5 to 0
Step3: WriteMemoryDWord(0xFED1F410, DWordData)     //Write back to memory
```

Note:

The system will be rebooted after user's setting + 2 seconds. 2 seconds added is Intel's limitation.

### ***Step2*** *Set Initial Value into Timer Register*

**Target: Set TCO Timer Initial Value (Offset 0x12)**

*Step1: WordData = ReadIOWord(0x472)* *//0x460+0x12*

*Step2: WordData = Set Bit[9:0]* *//0x000~0xFFF. 1 ticks = 0.6s*

*Step3: WriteIOWord(0x472,WordData)* *//Write back to IO*

Example:

If you want to reboot after 5 seconds, you should set WordData to 0x05.

5 - 2 = 3 //5 minus system's default 2 seconds leaves the real setting data.

3 / 0.6 = 5 //5 ticks

### ***Step3*** *Reload Timer Value into Register*

**Target: Reload Timer Initial Value to TCO_RLD Register (Offset 0x00)**

*Step1: WriteIOWord(0x460, 0x01)* *//Reload Timer*

### ***Step4*** *Start to Count*

**Target: Enable Time to count (Offset 0x08)**

*Step1: WordData = ReadIOWord(0x468)* *//0x460+0x08*

*Step2: WordData = WordData & 0xF7FF* *//Enabled to count*

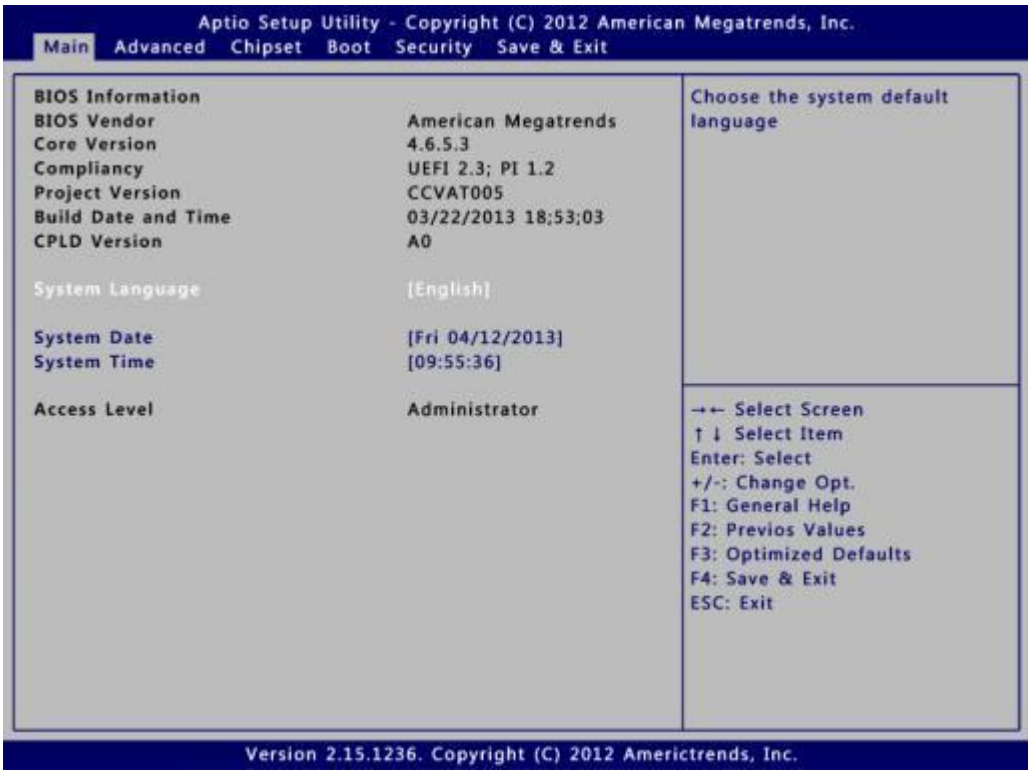
*Step3: WriteIOWord(0x468, WordData)* *// Write back to IO*

# V. SYSTEM BIOS

The system BIOS software is stored on EEPROM. The BIOS provides an interface to modify the configuration. When the battery is removed, all the parameters will be reset.
Turn on the computer and press <DEL> or <F2> to enter the setup screens.

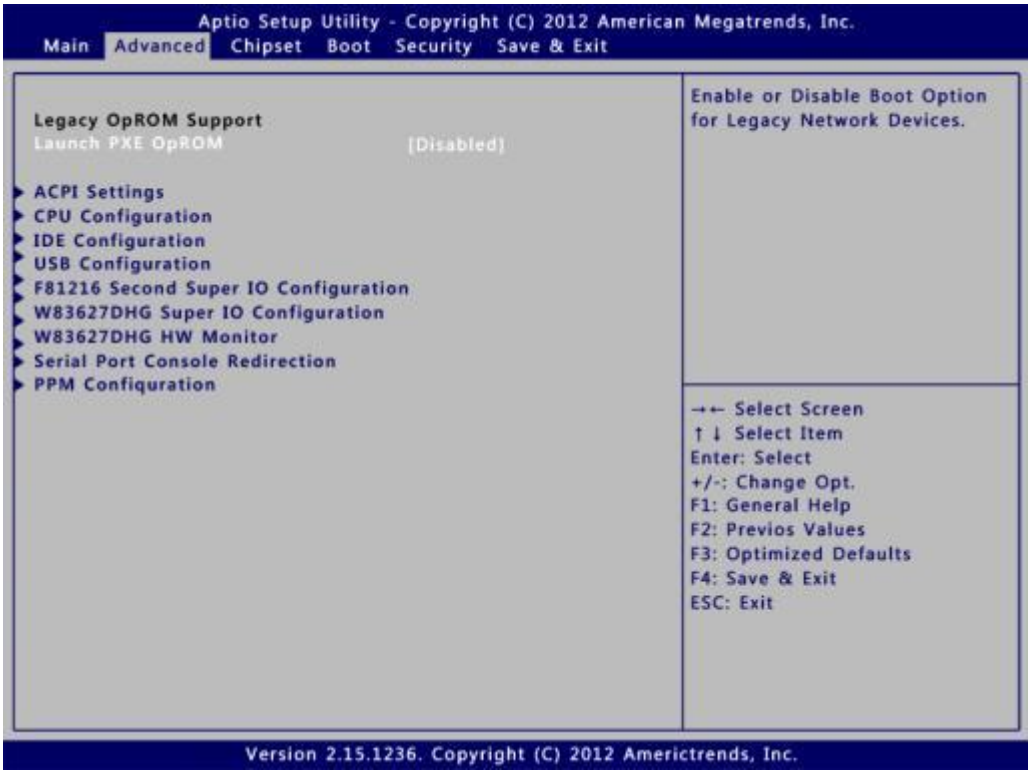
## 5.1 Main

The Main setup screen is showed as following when the setup utility is entered. System Date/Time is set up in the Main Menu.



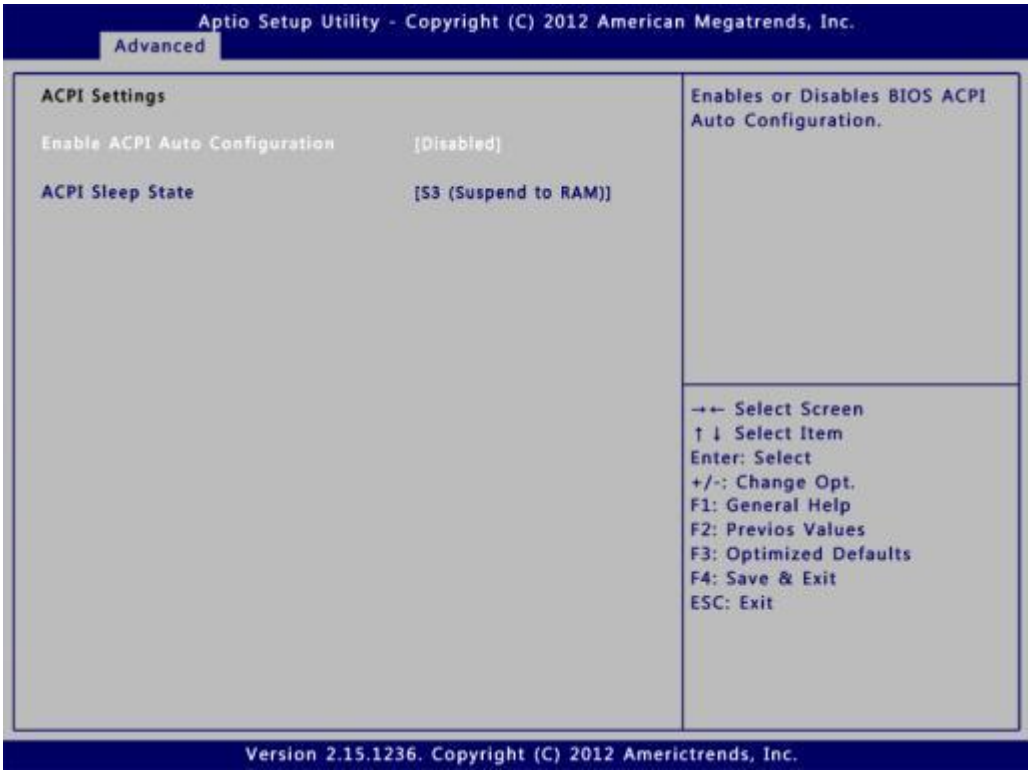

**System Language:** Choose the system default language
**System Date:** MM/DD/YYYY. Set the Date. Use Tab to switch between Date elements.
**System Time:** HH:MM:SS. Set the Time. Use Tab to switch between Time elements.

## 5.2 Advanced




**Launch PXE OpROM :** Enable or Disable Boot Option for Legacy Network Devices.

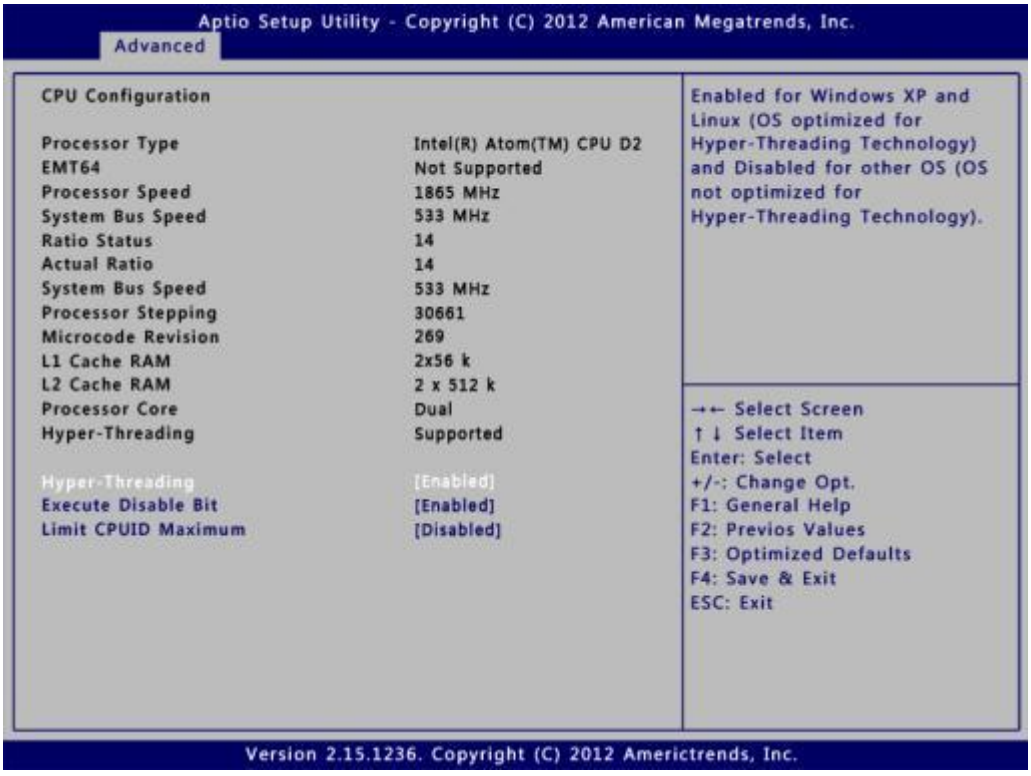
### 5.2.1 ACPI Settings




**Enable ACPI Auto Configuration:** Enable or Disable BIOS ACPI Auto Configuration.

**ACPI Sleep State:** Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Select between[Suspend Disabled], [S1 (CPU Stop Clock)] and [S3 (Suspend to RAM)].

## 5.2.2 CPU Configuration



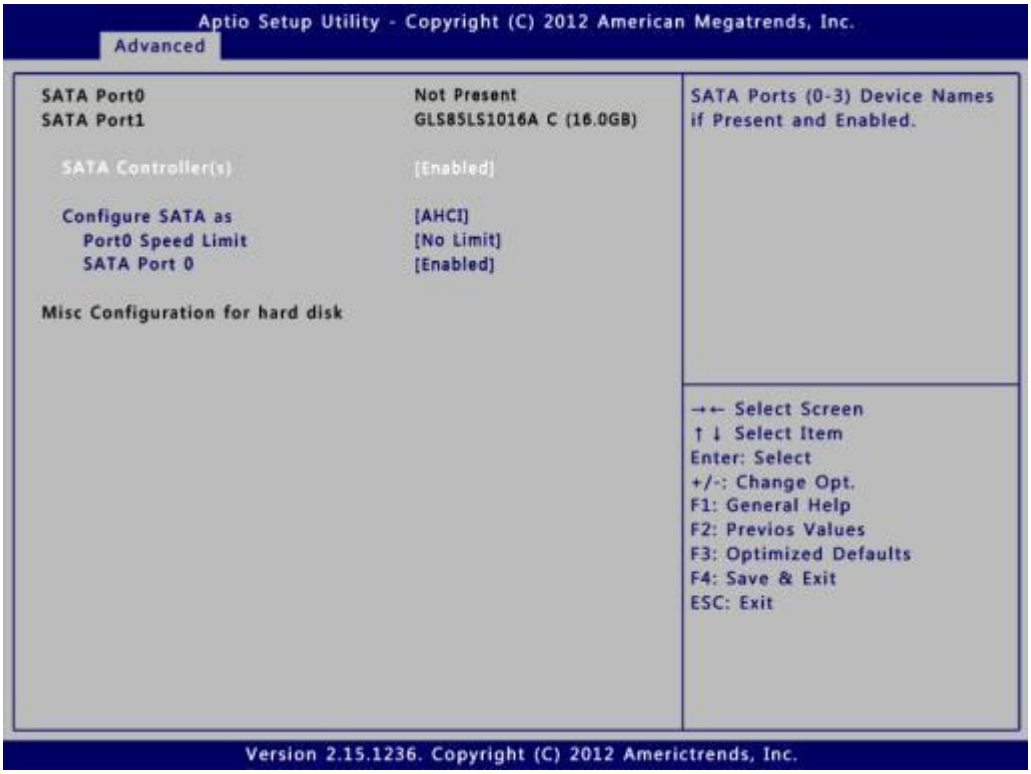

**Hyper-threading:** Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When disabled, only one thread per enabled core is enabled.

**Execute Disable Bit:** XP can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SusE Linux 9.2, RedHat Enterprise 3 Update 3.)

**Limit CPUID Maximum:** Disabled for Windows XP.

### 5.2.3 IDE Configuration

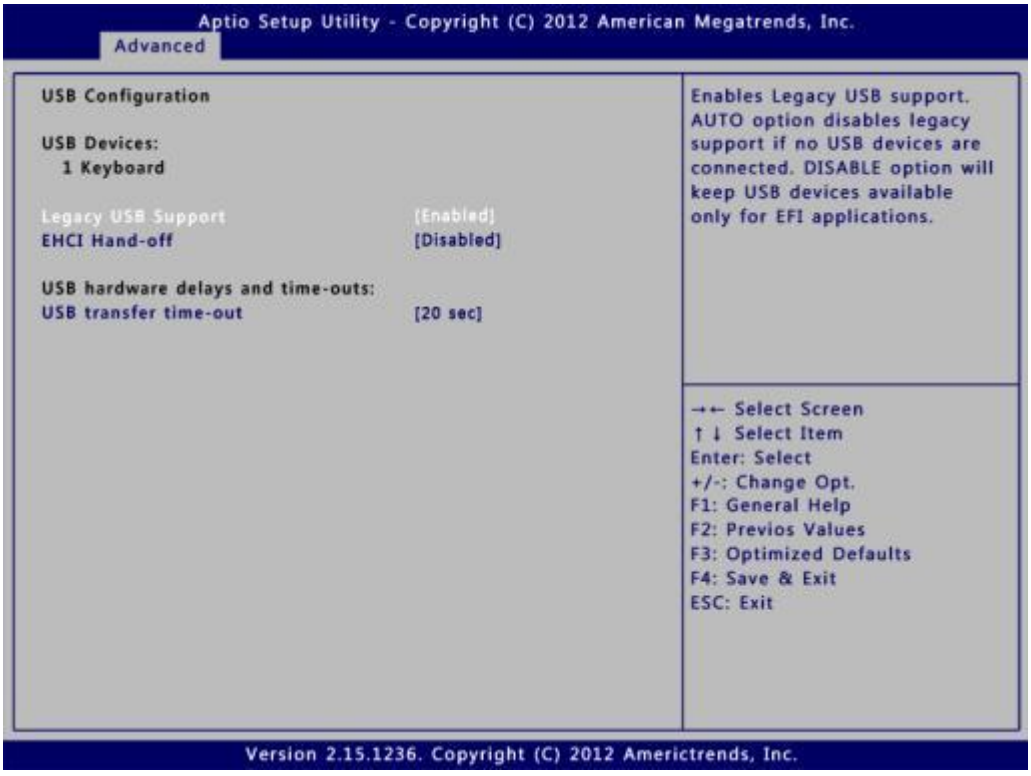
The BIOS automatically detects the presence of SATA device and the hardware installed in the SATA ports will be showed in the configuration. Each port can be enabled or disabled individually.




**Configure SATA as:** Select IDE or AHCI mode for SATA controller operations.

**Port0 Speed Limit:** Select between [No Limit], [GEN1 Rate] and [GEN2 Rate].

### 5.2.4 USB Configuration

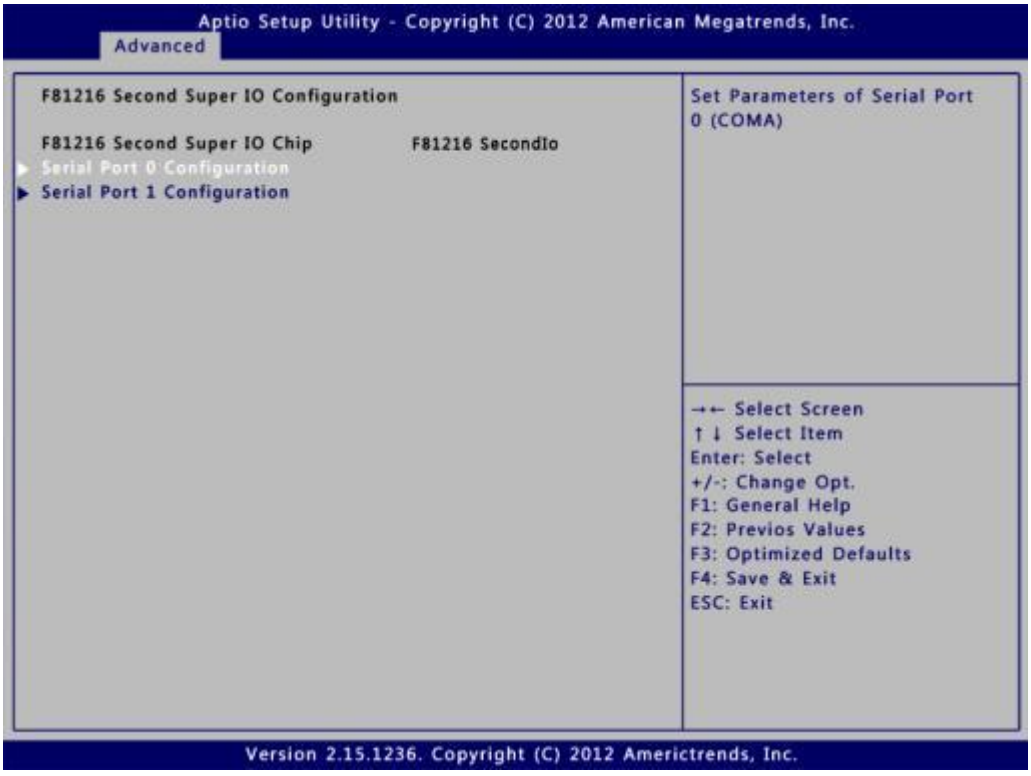



**Legacy USB Support:** AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

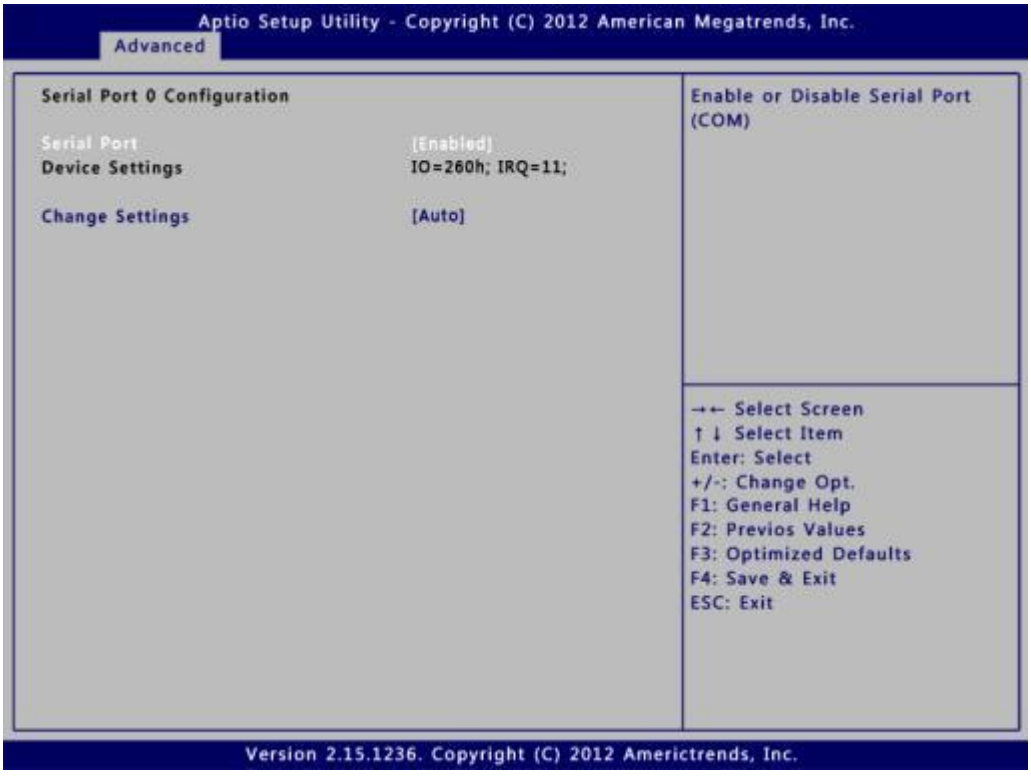
**EHCI Hand-off:** This is a workaround for OS without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

**USB transfer time-out:** Select the time-out value, [1 sec], [5 sec], [10 sec] or [20 sec], for Control, Bulk, and Interrupt transfers.

## 5.2.5 F81216 Second Super IO Configuration



#### 5.2.5.1 Serial Port0 Configuration




Each serial port could be enabled or disabled.

Serial Port 0 could change the setting to the following:

[Auto]

[IO=260h; IRQ=11;]

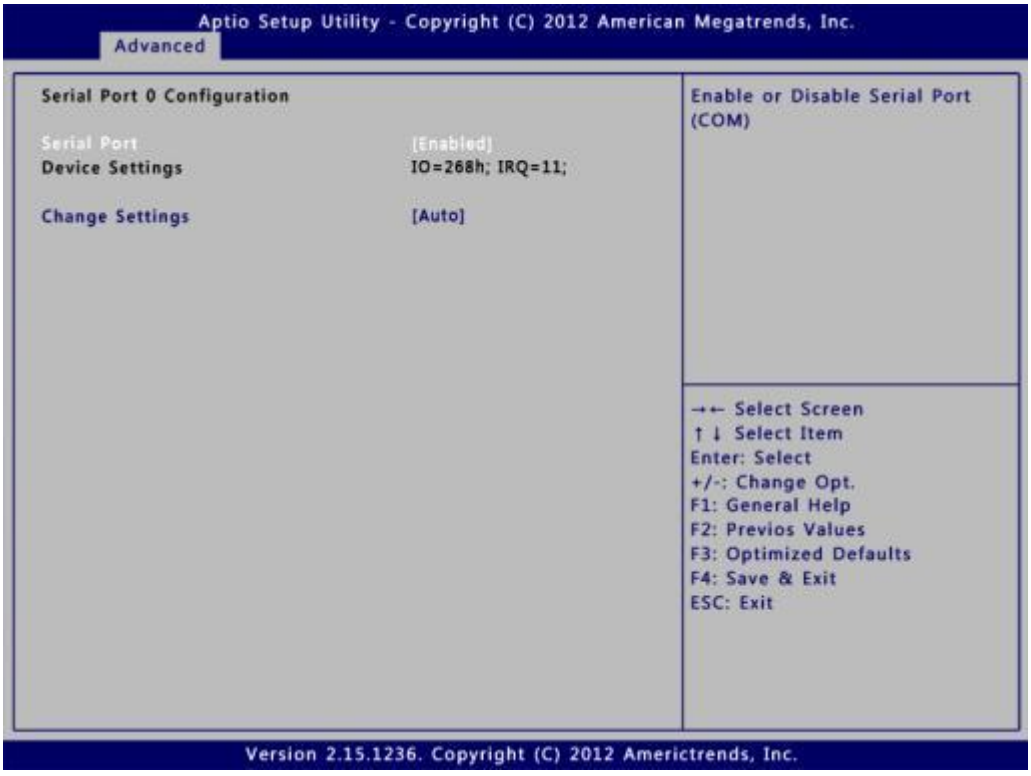
[IO=260h; IRQ=10,11,12;]

[IO=268h; IRQ=10,11,12;]

[IO=270h; IRQ=10,11,12;]

[IO=278h; IRQ=10,11,12;]

#### 5.2.5.1 Serial Port1 Configuration




Each serial port could be enabled or disabled.

Serial Port 1 could change the setting to:

[Auto]

[IO=268h; IRQ=11;]

[IO=260h; IRQ=10,11,12;]

[IO=268h; IRQ=10,11,12;]

[IO=270h; IRQ=10,11,12;]

[IO=278h; IRQ=10,11,12;]

### 5.2.6 W83627DHG Super IO Configuration

Two serial ports could be configured.

#### 5.2.6.1 Serial Port0 Configuration

Each serial port could be enabled or disabled.

Serial Port 0 could change the setting to the following:

[Auto]

[IO=3F8h; IRQ=4;]

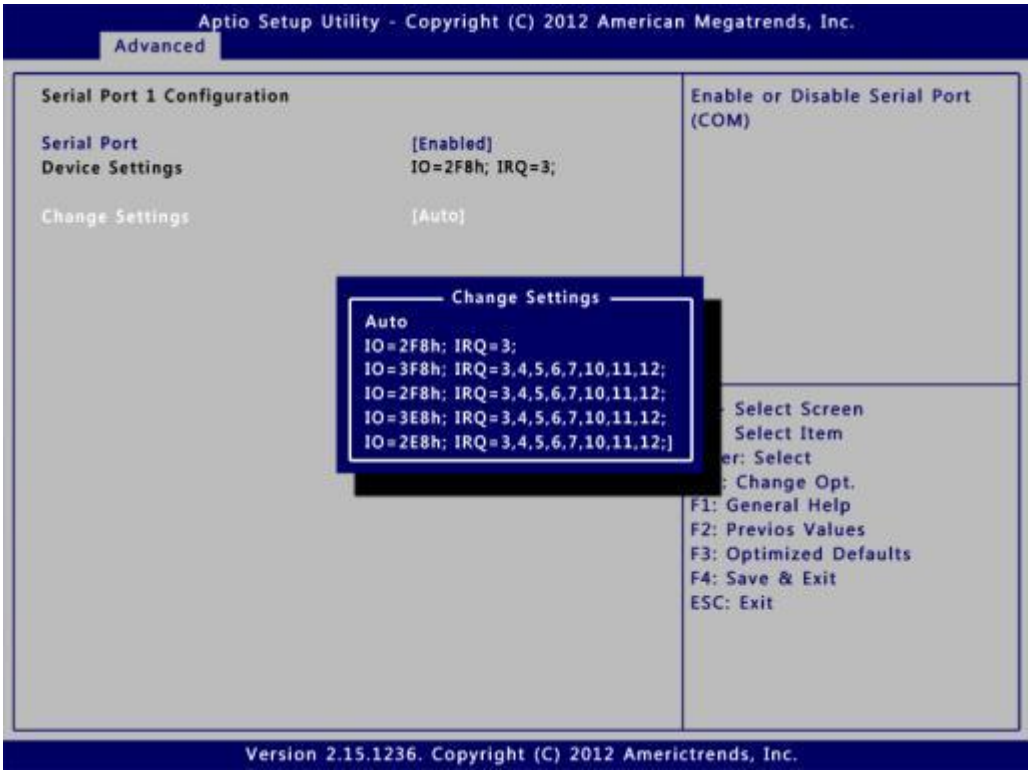
[IO=3F8h; IRQ=3,4,5,6,7,10,11,12;]

[IO=2F8h; IRQ=3,4,5,6,7,10,11,12;]

[IO=3E8h; IRQ=3,4,5,6,7,10,11,12;]

[IO=2E8h; IRQ=3,4,5,6,7,10,11,12;]

### 5.2.6.2 Serial Port1 Configuration




Each serial port could be enabled or disabled.

Serial Port 1 could change the setting to the following:

[Auto]

[IO=2F8h; IRQ=3;]

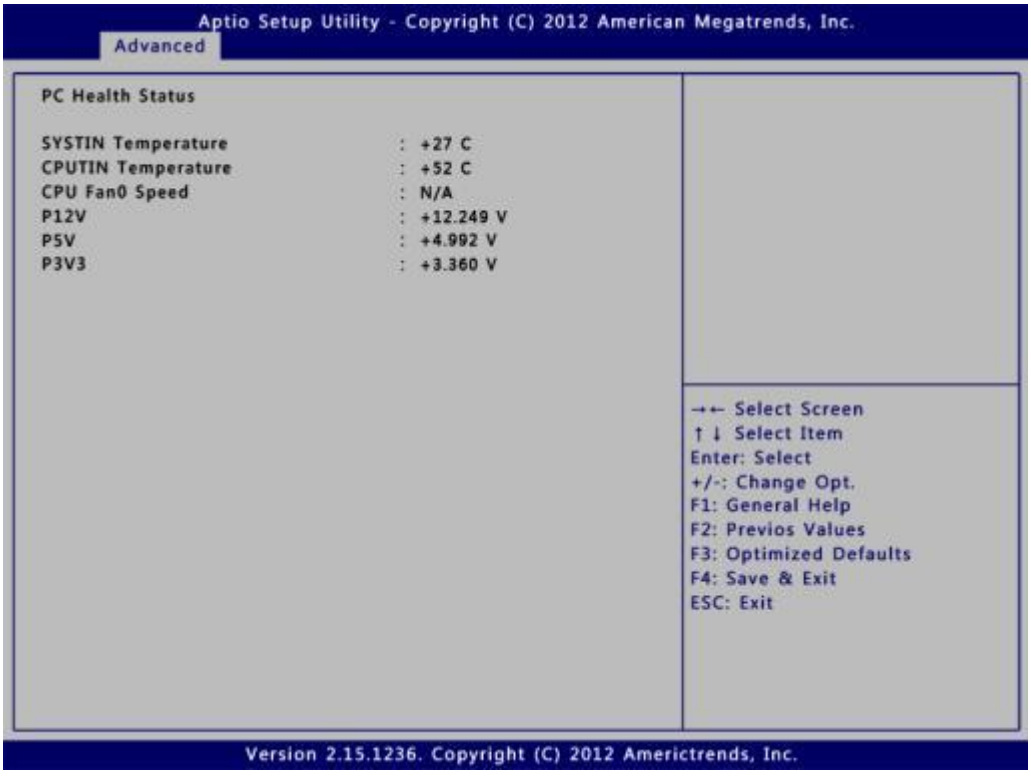
[IO=3F8h; IRQ=3,4,5,6,7,10,11,12;]

[IO=2F8h; IRQ=3,4,5,6,7,10,11,12;]

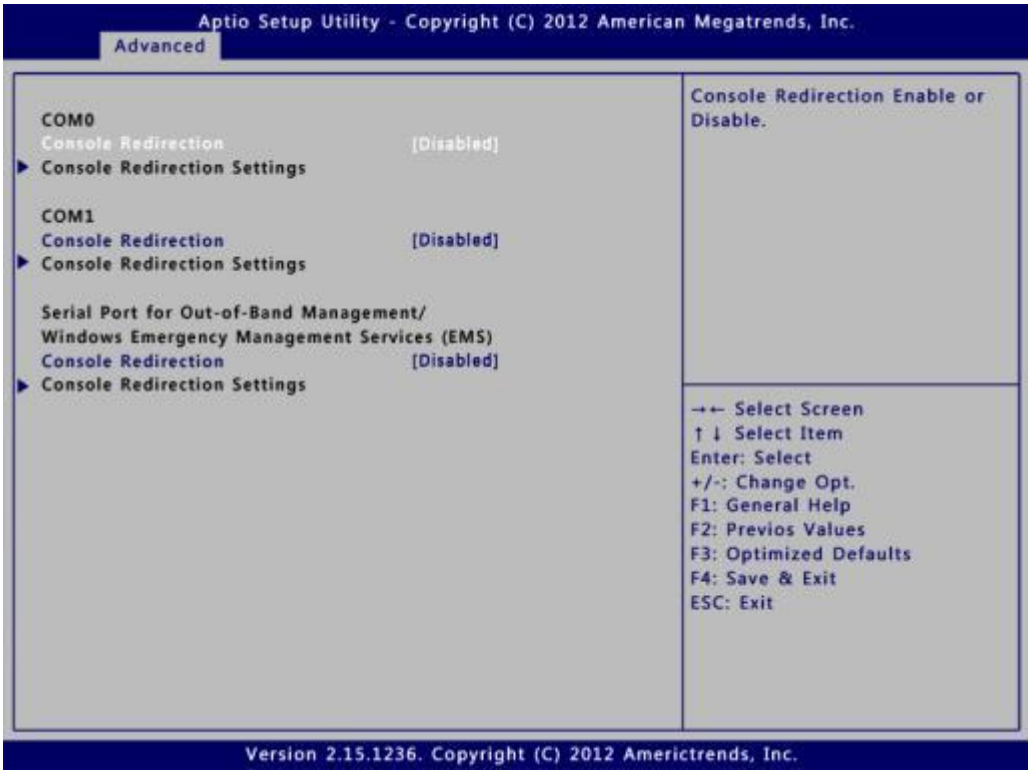
[IO=3E8h; IRQ=3,4,5,6,7,10,11,12;]

[IO=2E8h; IRQ=3,4,5,6,7,10,11,12;]

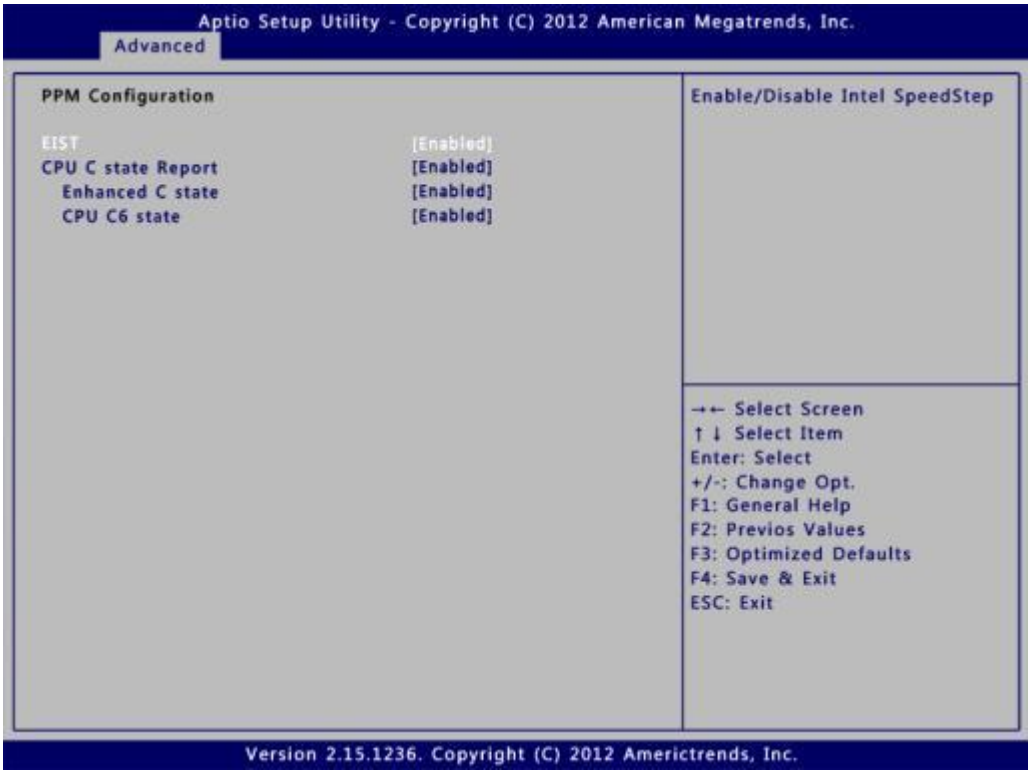
## 5.2.7 W83627DHG HW Hardware (Pc Health Status)



## 5.2.8 Serial Port Console Redirection



## 5.2.9 PPM Configuration

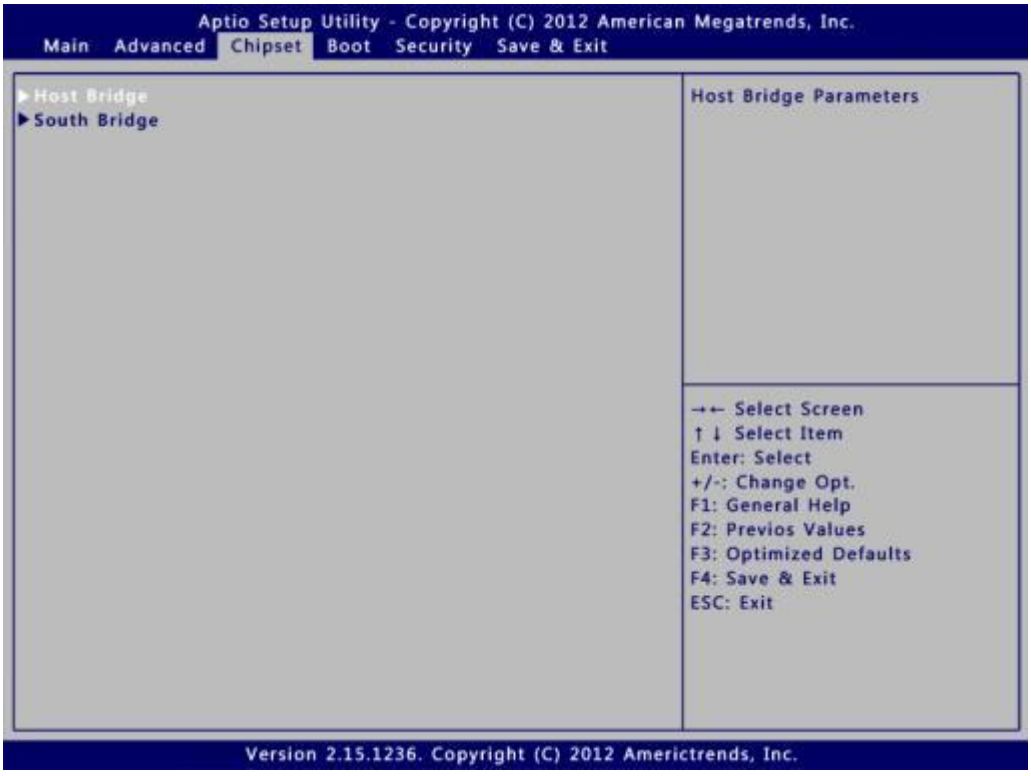



**CPU C state Report:** Enable or Disable CPU C state report to OS
If this option is set to “enabled”(default is set to disabled), it will expand two sub-options:

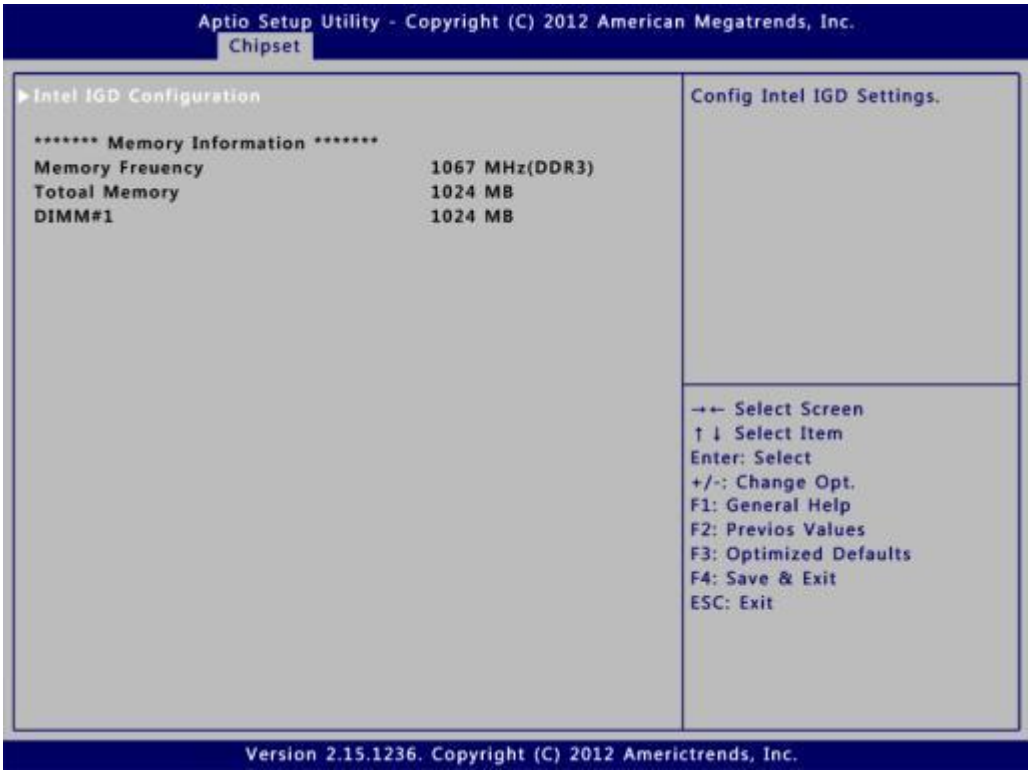
**Enhanced C state:** Enable or Disable Enhanced CPU C state

**CPU C6 state:** Enable or Disable CPU c6 state.

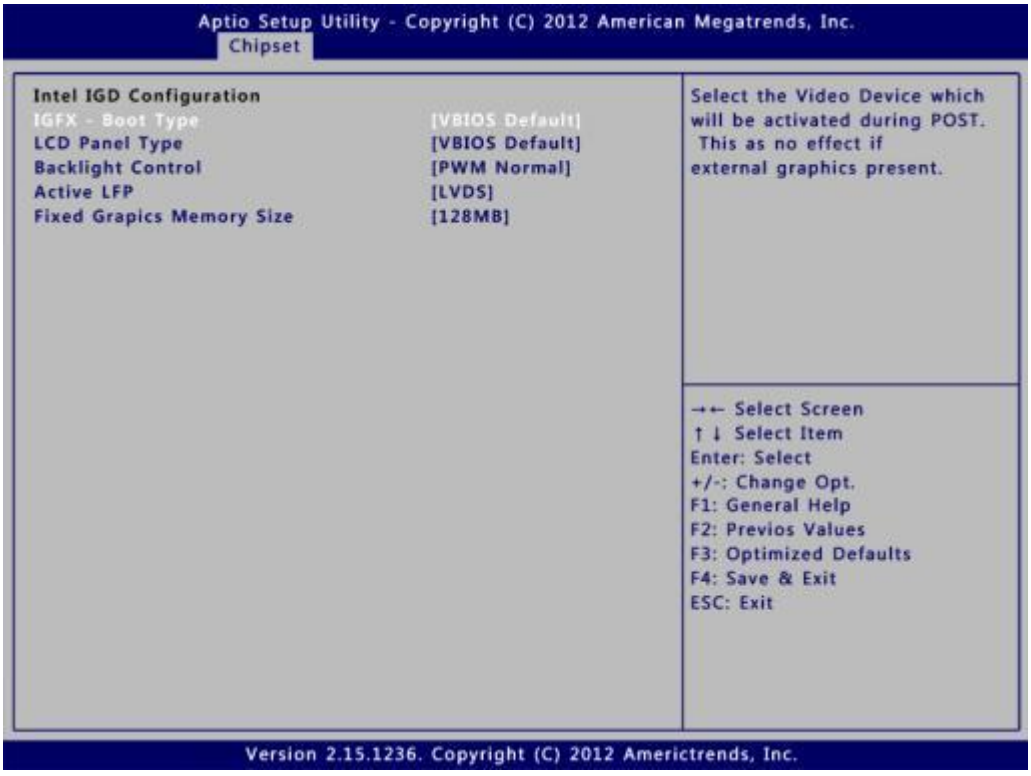
## 5.3 Chipset


Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Host Bridge
South Bridge
Host Bridge Parameters
→← Select Screen
↑ ↓ Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previos Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1236. Copyright (C) 2012 Americtrends, Inc.

### 5.3.1 Host Bridge



#### 5.3.1.1 Intel IGD Configuration




**IGFX – Boot Type:** Select the Video Device which will be activated during POST. This has no effect if external graphics present. Select between [VBIOS Default], [CRT], [LFP], [EFP], [CRT+EFP] and [LFP+EFP].

**LCD Panel Type:** Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item: [VBIOS Default], [640x480 LVDS], [800x600 LVDS], [1024x768 LVDS], [1280x1024 LVDS], [1366x768 LVDS] or [1280x800 LVDS].

**Backlight Control:** Select between [PWM Inverted] and [PWM Normal].

**Active LFP:** Select the Active LFP Configuration.

No LVDS: VBIOS does not enable LVDS.

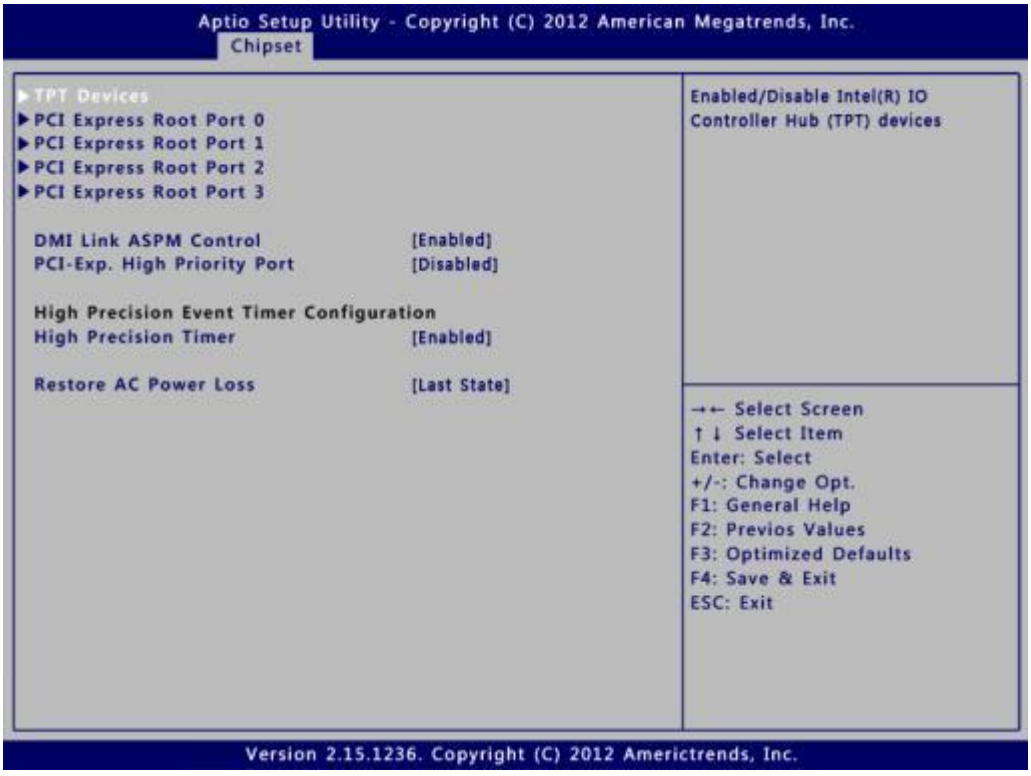
Int-LVDS: VBIOS enables LVDS driver by Integrated encoder.

SDVO LVDS: VBIOS enables LVDS driver by SDVO encoder.

eDP Port-A: LFP Driven by Int-DisplayPort encoder from Port-A.

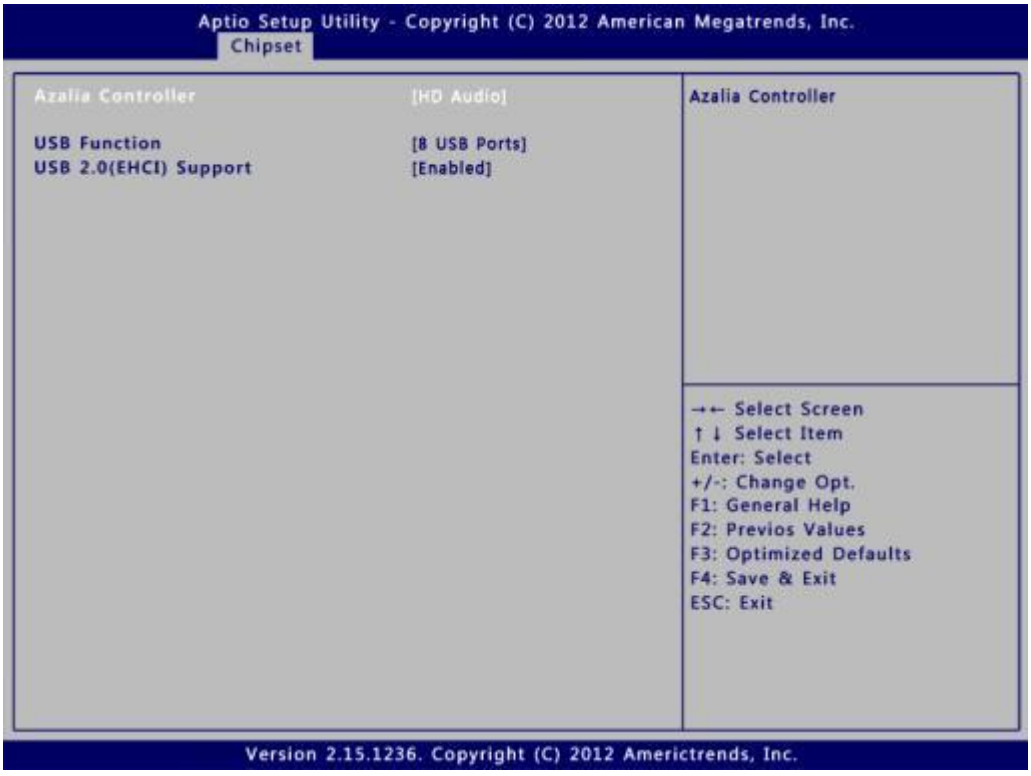
**Fixed Graphics Memory Size:** Select Fixed Graphics Memory Size between [128MB] and [256MB].

### 5.3.2 South Bridge




**TPT Devices:** Enable/Disable Intel(R) IO Controller Hub (TPT) devices.
**DMI Link ASPM Control:** The control of Active State Power Management on both NB side and SB side of the DMI Link.
**PCI-Exp. High Priority Port:** Select a PCI Express High Priority Port to [Disabled], [Port 0], [Port 1], [Port 2] or [Port 3].
**High Precision Timer:** [Enable] or [Disable]
**Restore AC Power Loss:** Select between [Always OFF], [Always ON] and [Last State] when power is re-applied after a power failure.

#### 5.3.2.1 **TPT Devices**



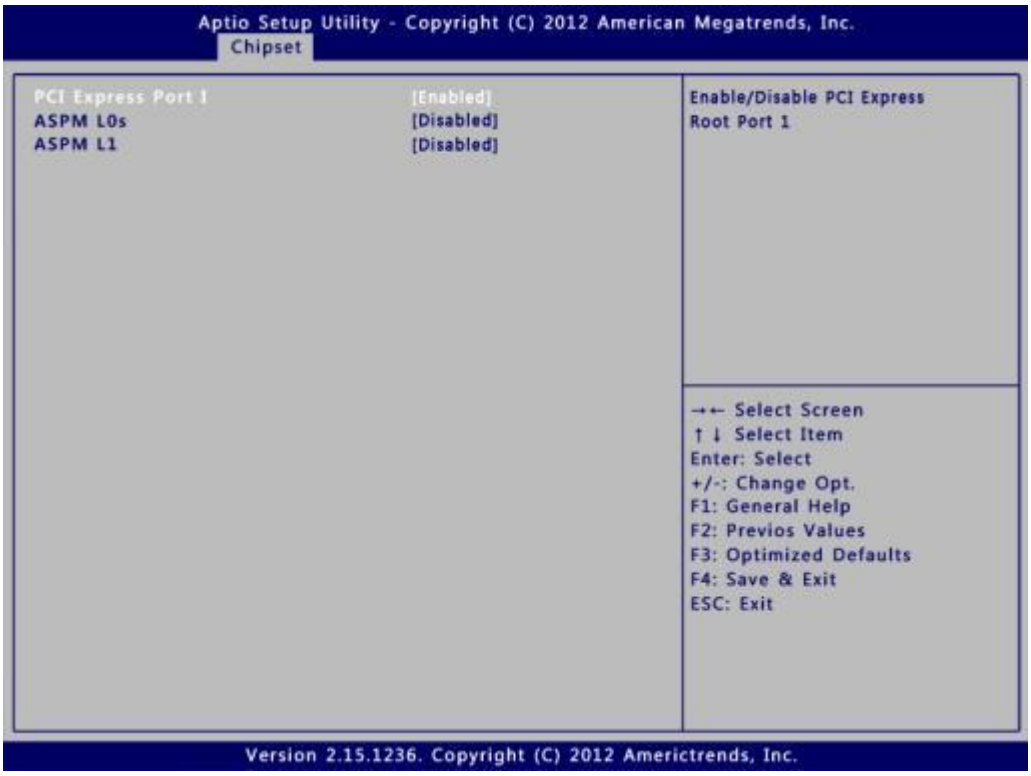

**Azalia Controller:** Select between [Disabled] and [HD Audio]

**USB Function**: Disable or enable USB Function.

**USB 2.0(EHCI) Support:** Enable or Disable USB2.0 (EHCI) Support.

#### 5.3.2.2 PCI Express Root Port Configuration

Each PCI Express Port from 0 to 3 can be setup.

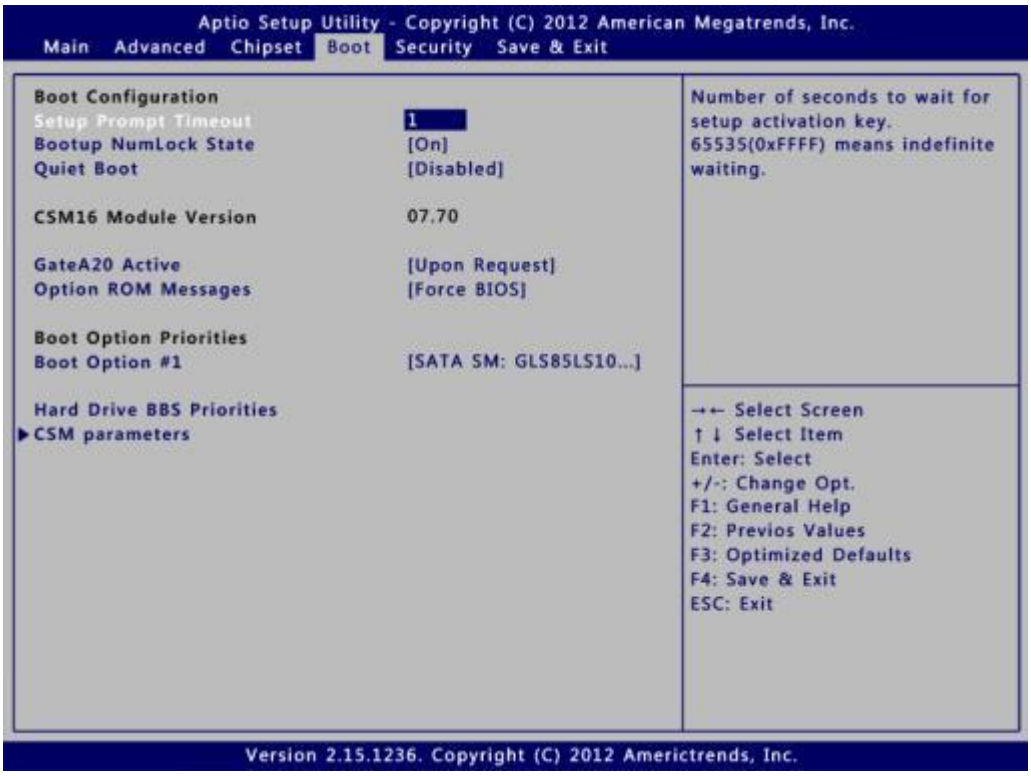



Each PCI Express Root Port can be enabled or disabled individually.

**ASPM L0s:** [Disabled], [Root Port Only], [Endpoint Port Only] or [Both Root And Endpoint Ports]

**ASPM L1:** [Disabled] or [Enabled]

# 5.4 Boot




**Boot Configuration:** Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.

**Bootup NumLock State:** Select [Enable] or [Disable] for the keyboard NumLock state.

**Quiet Boot:** Enables or disables Quiet Boot option.

**GateA20 Active:**

[Upon Request] – GA20 can be disabled using BIOS services.

[Always] – do not allow disabling GA20; this option is useful wen any RT code is executed above 1MB.

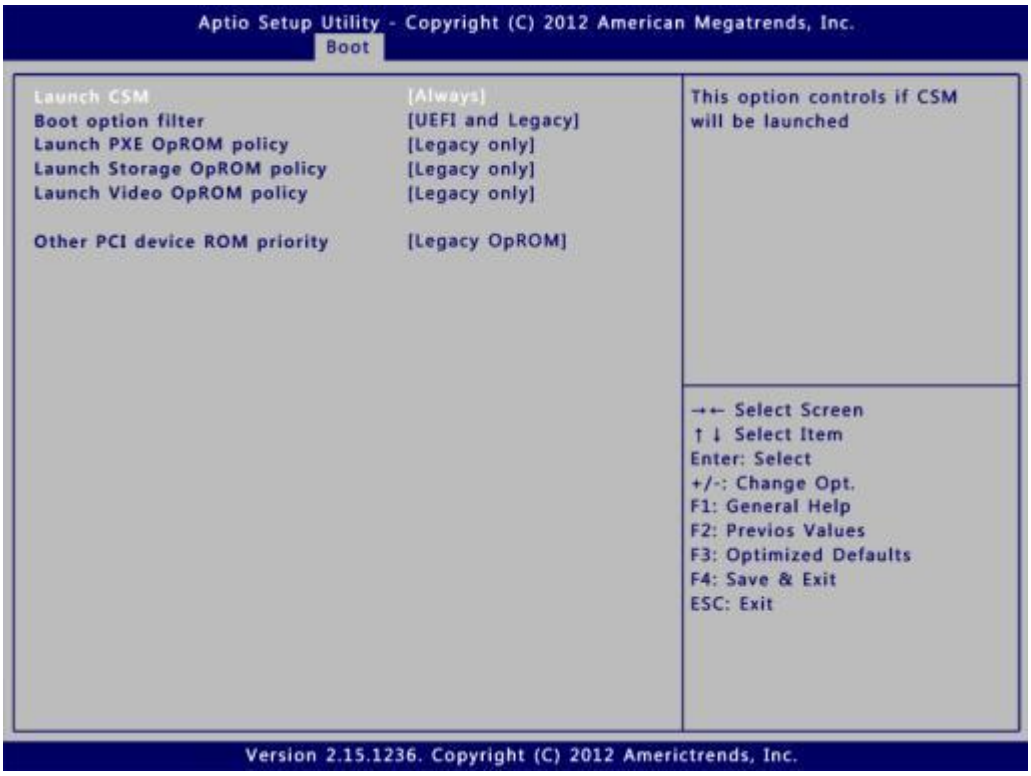
**Option ROM Message:** Set display mode [Force BIOS] or [Keep Current] for Option ROM.

**Boot Option #1:** Set the system boot order.

**Hard Drive BBS Priorities:** Set the order of the legacy devices in this group.

### 5.4.1 CSM parameters

OpROM execution, boot options filter, etc.

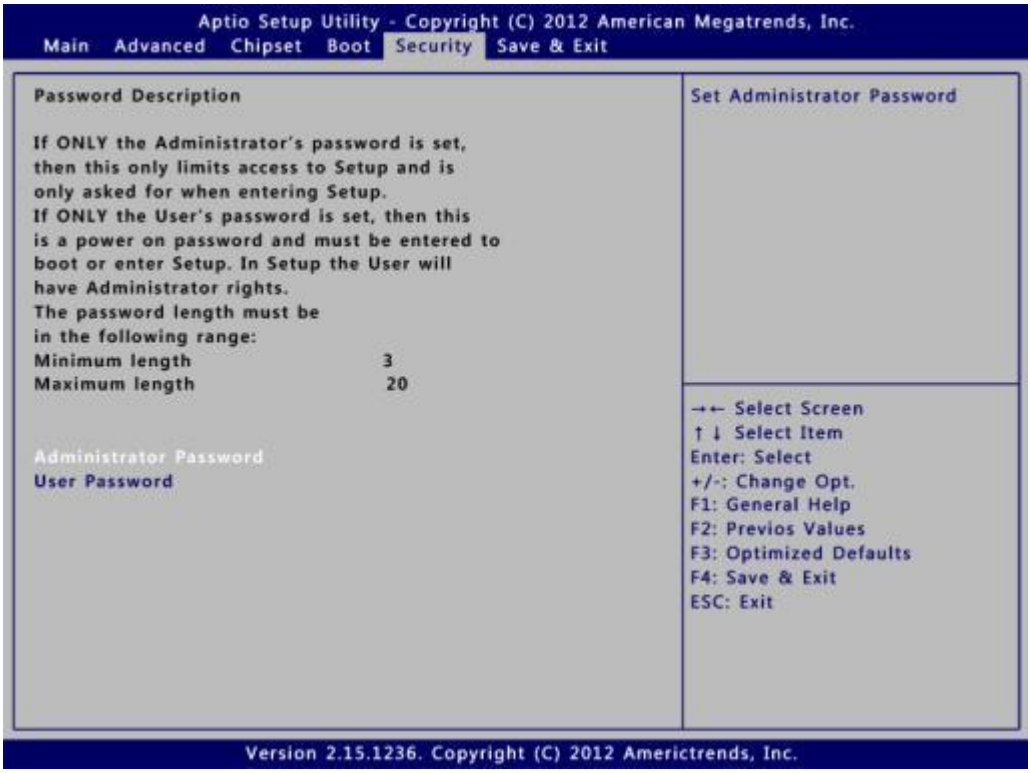



**Launch CSM:** This option controls if CSM will be launched always or never.
**Boot option filer:** This option controls what devices system can boot to [UEFI and Legacy], [Legacy only] or [UEFI only].
**Launch PXE OpROM policy:** This controls the execution of UEFI and Legacy PXE OpROM, [Do not launch], [UEFI only] or [Legacy only].
**Launch Storage OpROM policy:** This controls the execution of UEFI and Legacy Storage OpROM, [Do not launch], [UEFI only] or [Legacy only].
**Launch Video OpROM policy:** This controls the execution of UEFI and Legacy Video OpROM, [Do not launch], [UEFI only] or [Legacy only].
Other PCI device ROM priority: For PCI devices other than Network, Mass storage or Video defines which OpROM to launch, [UEFI OpROM] or [Legacy OpROM].

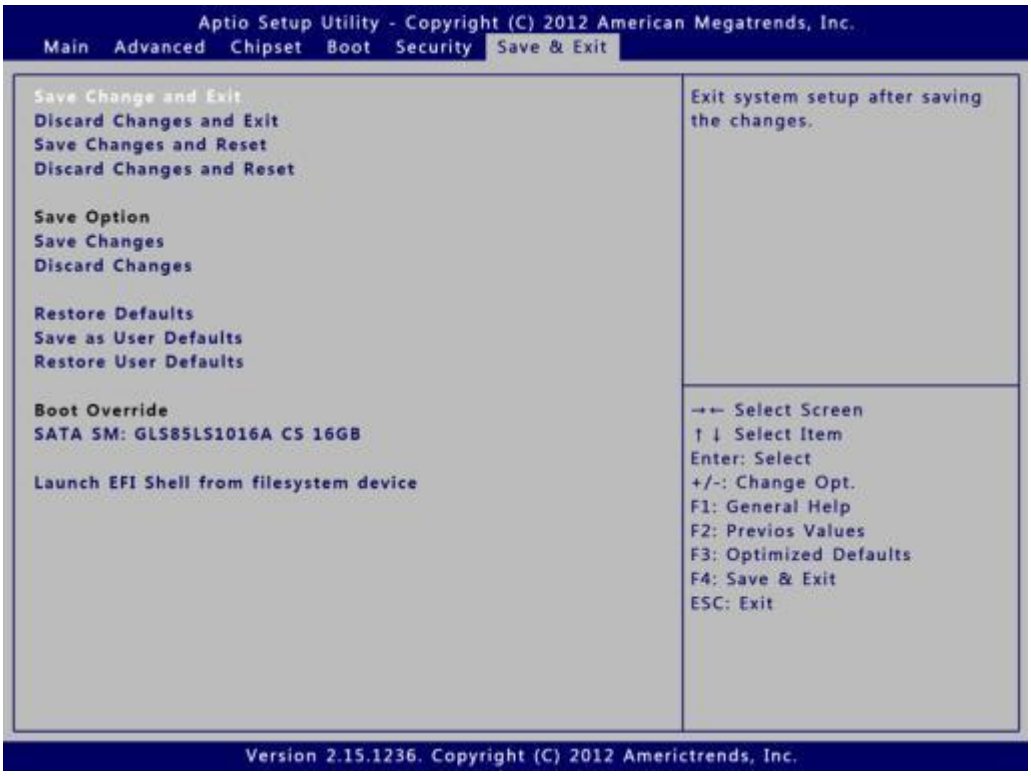
## 5.5 Security

Administrator's and User's passwords could be set.

If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup, the user will have administrator rights. The minimum length of the password is 3 and the maximum length is 20.



## 5.6 Save and Exit

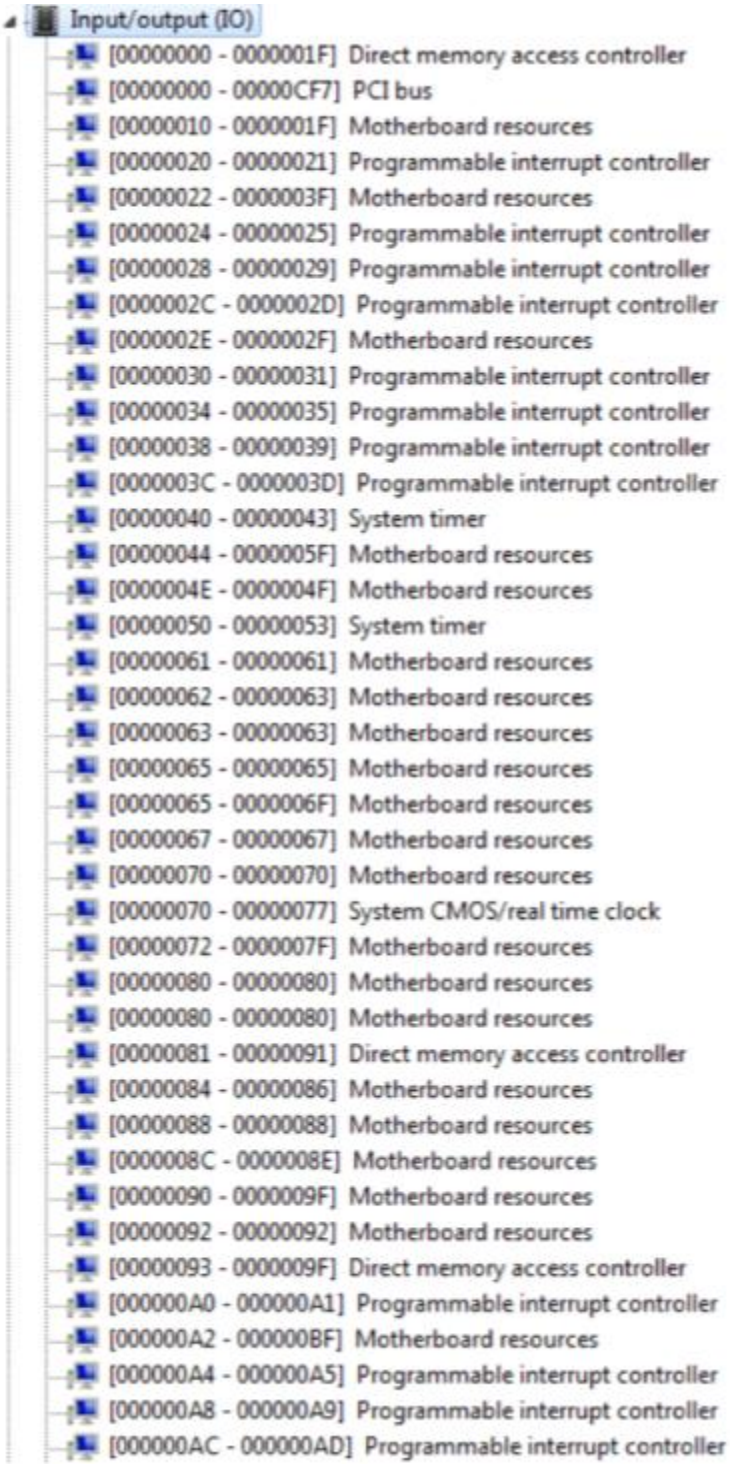


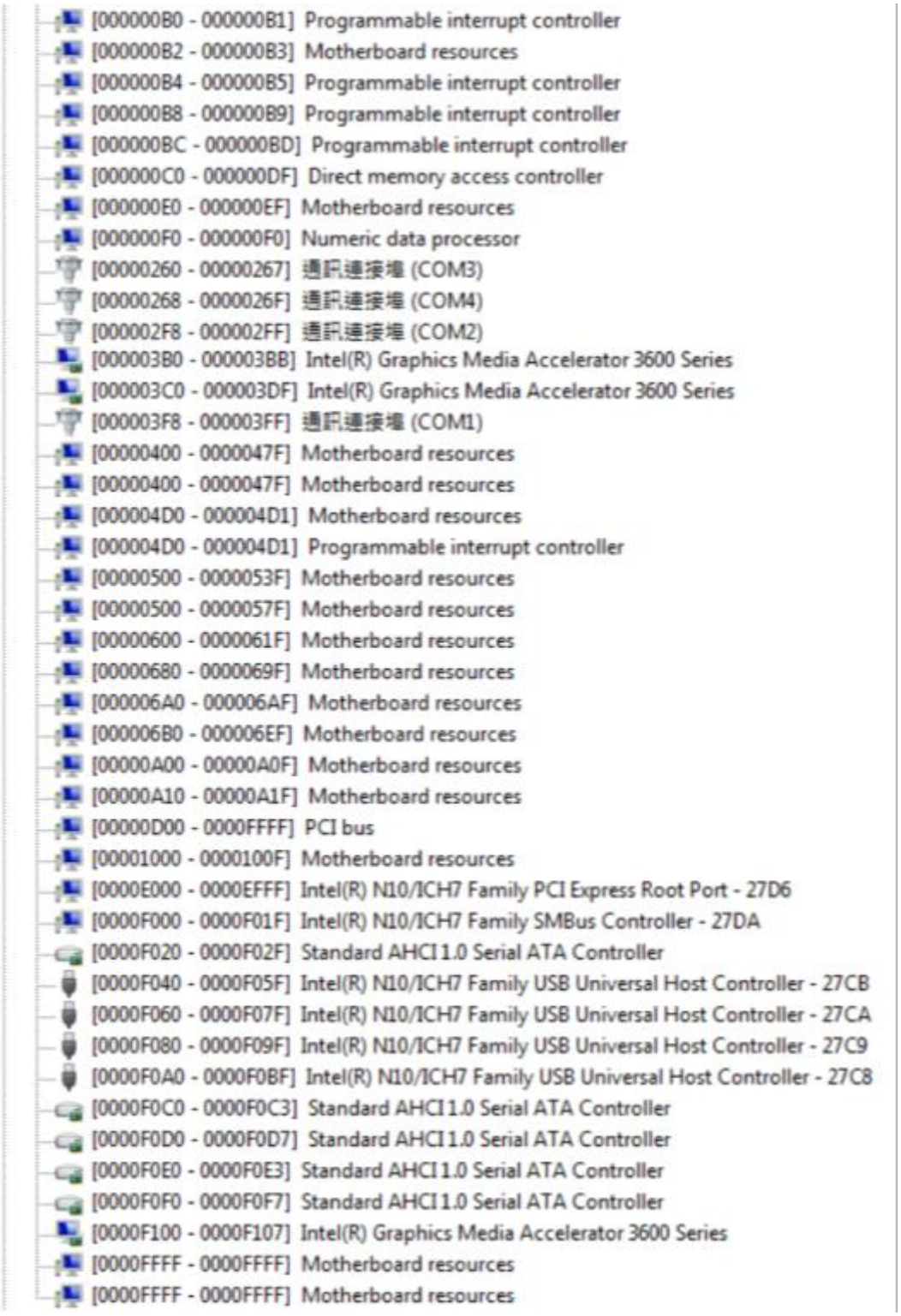

**Save Changes and Exit:** Exit system setup after saving the changes.
**Discard Changes and Exit:** Exit system setup without saving any changes.
**Save Changes and Reset:** Reset the system after saving the changes.
**Discard Changes and Reset:** Reset system setup without saving any changes.
**Save Changes:** Save Changes done so far to any of the setup options.
**Discard Changes:** Discard Changes done so far to any of the setup options.
**Restore Defaults:** Restore/Load Default values for all the setup options.
**Save as User Defaults:** Save the changes done so far as user Defaults.
**Restore user Defaults:** Restore the User Defaults to all the setup options.
**Launch EFI Shell from filesystem device:** Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available filesystem devices.

# VI. Address Map

## 6.1 I/O Port Address Map

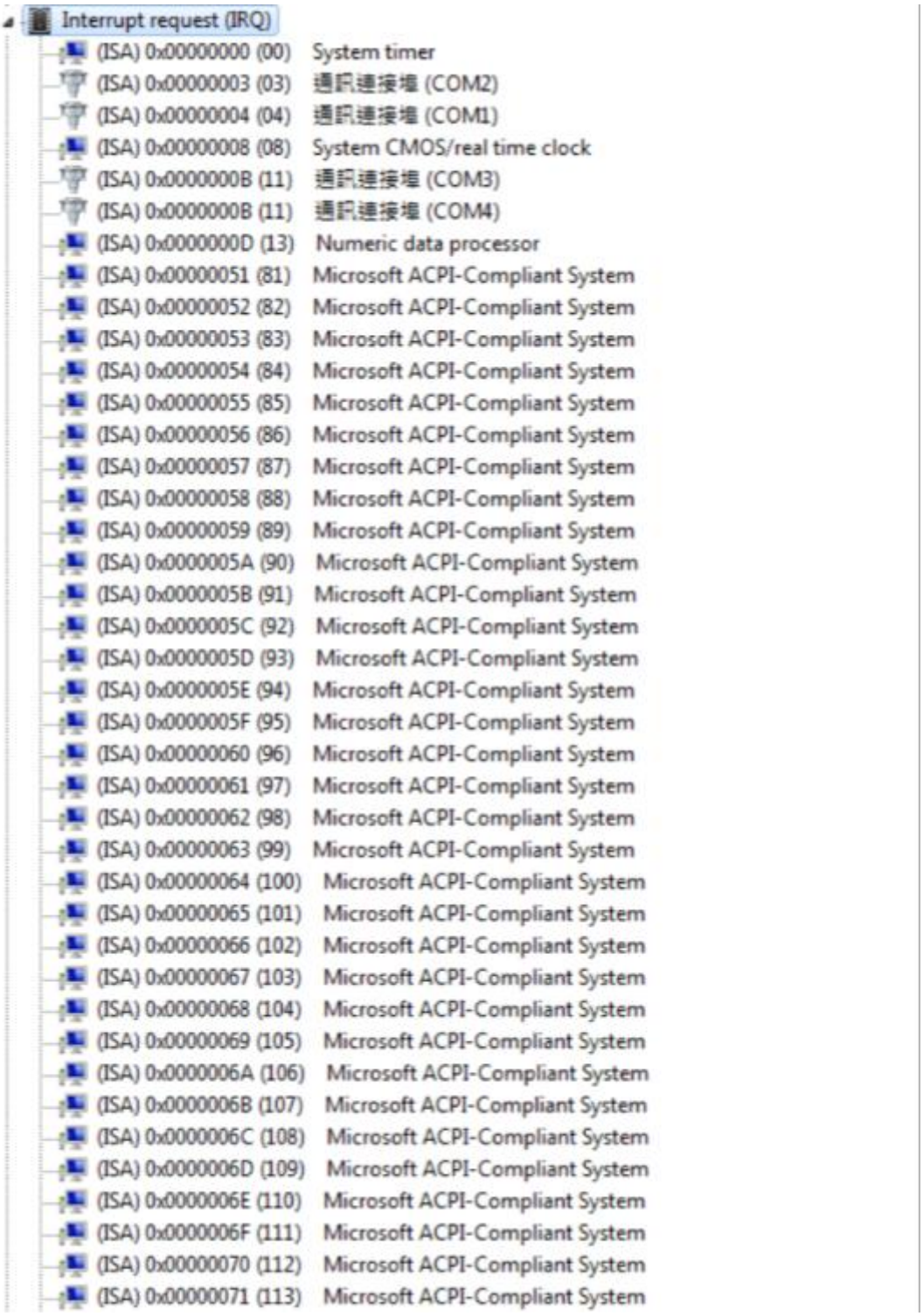
The assignment of the I/O port addresses for the CT-CCVAX with CT-BTA01 carrier board under Windows® 7 Ultimate/64bit are shown below.



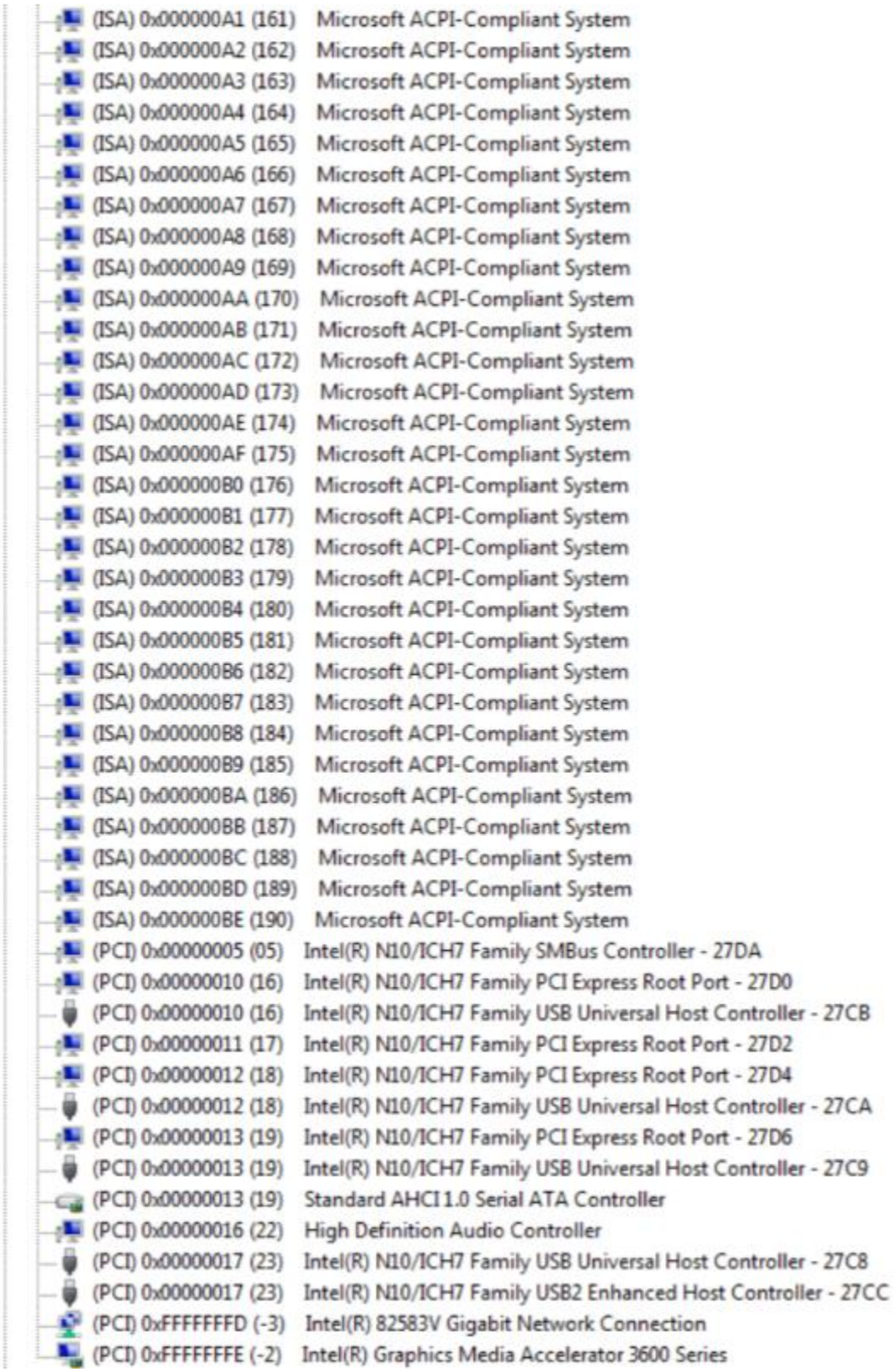

[000000B0 - 000000B1] Programmable interrupt controller
[000000B2 - 000000B3] Motherboard resources
[000000B4 - 000000B5] Programmable interrupt controller
[000000B8 - 000000B9] Programmable interrupt controller
[000000BC - 000000BD] Programmable interrupt controller
[000000C0 - 000000DF] Direct memory access controller
[000000E0 - 000000EF] Motherboard resources
[000000F0 - 000000F0] Numeric data processor
[00000260 - 00000267] 通訊連接埠 (COM3)
[00000268 - 0000026F] 通訊連接埠 (COM4)
[000002F8 - 000002FF] 通訊連接埠 (COM2)
[000003B0 - 000003BB] Intel(R) Graphics Media Accelerator 3600 Series
[000003C0 - 000003DF] Intel(R) Graphics Media Accelerator 3600 Series
[000003F8 - 000003FF] 通訊連接埠 (COM1)
[00000400 - 0000047F] Motherboard resources
[00000400 - 0000047F] Motherboard resources
[000004D0 - 000004D1] Motherboard resources
[000004D0 - 000004D1] Programmable interrupt controller
[00000500 - 0000053F] Motherboard resources
[00000500 - 0000057F] Motherboard resources
[00000600 - 0000061F] Motherboard resources
[00000680 - 0000069F] Motherboard resources
[000006A0 - 000006AF] Motherboard resources
[000006B0 - 000006EF] Motherboard resources
[00000A00 - 00000A0F] Motherboard resources
[00000A10 - 00000A1F] Motherboard resources
[00000D00 - 0000FFFF] PCI bus
[00001000 - 0000100F] Motherboard resources
[0000E000 - 0000EFFF] Intel(R) N10/ICH7 Family PCI Express Root Port - 27D6
[0000F000 - 0000F01F] Intel(R) N10/ICH7 Family SMBus Controller - 27DA
[0000F020 - 0000F02F] Standard AHCI 1.0 Serial ATA Controller
[0000F040 - 0000F05F] Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CB
[0000F060 - 0000F07F] Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CA
[0000F080 - 0000F09F] Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C9
[0000F0A0 - 0000F0BF] Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C8
[0000F0C0 - 0000F0C3] Standard AHCI 1.0 Serial ATA Controller
[0000F0D0 - 0000F0D7] Standard AHCI 1.0 Serial ATA Controller
[0000F0E0 - 0000F0E3] Standard AHCI 1.0 Serial ATA Controller
[0000F0F0 - 0000F0F7] Standard AHCI 1.0 Serial ATA Controller
[0000F100 - 0000F107] Intel(R) Graphics Media Accelerator 3600 Series
[0000FFFF - 0000FFFF] Motherboard resources
[0000FFFF - 0000FFFF] Motherboard resources

## 6.2 Interrupt Controller (IRQ) Map

The interrupt controller map for the CT-CCVAX with the CT-BTA01 carrier board under Windows® 7 Ultimate/64bit are as shown below.

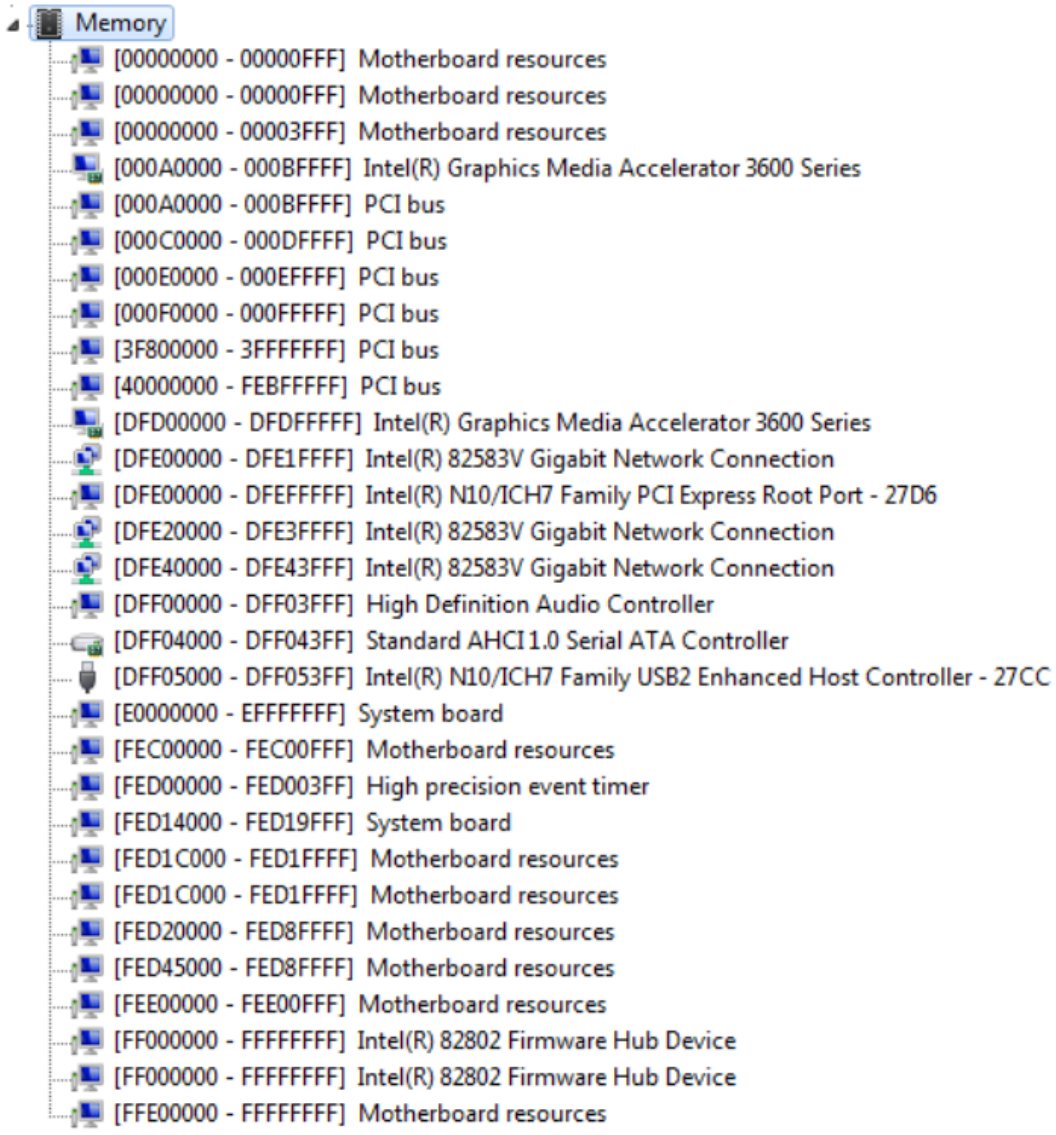


(ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115) Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116) Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
(ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
(ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
(ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
(ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
(ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
(ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
(ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
(ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
(ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
(ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
(ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System


(ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
(ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
(ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
(ISA) 0x000000A8 (168) Microsoft ACPI-Compliant System
(ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
(ISA) 0x000000AA (170) Microsoft ACPI-Compliant System
(ISA) 0x000000AB (171) Microsoft ACPI-Compliant System
(ISA) 0x000000AC (172) Microsoft ACPI-Compliant System
(ISA) 0x000000AD (173) Microsoft ACPI-Compliant System
(ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
(ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
(ISA) 0x000000B0 (176) Microsoft ACPI-Compliant System
(ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System
(ISA) 0x000000B2 (178) Microsoft ACPI-Compliant System
(ISA) 0x000000B3 (179) Microsoft ACPI-Compliant System
(ISA) 0x000000B4 (180) Microsoft ACPI-Compliant System
(ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
(ISA) 0x000000B6 (182) Microsoft ACPI-Compliant System
(ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
(ISA) 0x000000B8 (184) Microsoft ACPI-Compliant System
(ISA) 0x000000B9 (185) Microsoft ACPI-Compliant System
(ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
(ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
(ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
(ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
(ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
(PCI) 0x00000005 (05) Intel(R) N10/ICH7 Family SMBus Controller - 27DA
(PCI) 0x00000010 (16) Intel(R) N10/ICH7 Family PCI Express Root Port - 27D0
(PCI) 0x00000010 (16) Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CB
(PCI) 0x00000011 (17) Intel(R) N10/ICH7 Family PCI Express Root Port - 27D2
(PCI) 0x00000012 (18) Intel(R) N10/ICH7 Family PCI Express Root Port - 27D4
(PCI) 0x00000012 (18) Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CA
(PCI) 0x00000013 (19) Intel(R) N10/ICH7 Family PCI Express Root Port - 27D6
(PCI) 0x00000013 (19) Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C9
(PCI) 0x00000013 (19) Standard AHCI 1.0 Serial ATA Controller
(PCI) 0x00000016 (22) High Definition Audio Controller
(PCI) 0x00000017 (23) Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C8
(PCI) 0x00000017 (23) Intel(R) N10/ICH7 Family USB2 Enhanced Host Controller - 27CC
(PCI) 0xFFFFFFFD (-3) Intel(R) 82583V Gigabit Network Connection
(PCI) 0xFFFFFFFE (-2) Intel(R) Graphics Media Accelerator 3600 Series

## 6.3 Memory Map

The memory map of DRAM for the CT-CCVAX with CT-BTA01 carrier board under Windows® 7 Ultimate/64bit are shown below.



# VII. Electrical Specification

## 7.1 Input Power

The carrier board for the CT-CCVAX shall supply a single main power rail with a nominal value of +4.75~+14.7V and +3V RTC power.