



DMP ELECTRONIC INC.

8F, No.12 Wu-Quan 7 Rd., Wu-Gu Industrial Park,
Wu Gu Xiang, Taipei #248, Taiwan, R.O.C.
TEL: +886-2-2298-0770 FAX:+886-2-2299-1833

EmbedDisk DDOM-SST Datasheet

Version 2.0
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A. Product Information

Dependable and secure

Designed with advanced IDE flash controller technology, EmbedDisk is 100% compatible with the standard IDE/ATA storage interface without the need for special device driver. This advanced multi-tasking IDE flash controller's integrated error-detection, error-correction, re-mapping and wear-leveling technologies with power hold-up circuit greatly improves data reliability. Its low-power requirement, advanced PIO modes, multi-sector transfer support and LBA addressing can satisfy application with high performance and reliability requirements.

Anti Shock & Anti Vibration

Using advanced solid-state storage technology, without moving parts, EmbedDisk is able to perform all of its designated function without being affected by shock and vibration.

Wide Operating Temperature

EmbedDisk is designed to support commercial and industrial applications operating in environment exposed to extreme temperature range. The EmbedDisk DDOM series supports **-40°C to +85°C** operating temperature.

B. Features

- -40 °C to +85°C extreme temp range
- Power & Active LEDs, easy to check work status
- RoHS Compliant
- Industrial grade connector, avoid inaccuracy connection
- Write Protect
- Low power operation
- Fixed hole layout
- Unitized 44 pin IDE
- ECC for exceptional data reliability
- Completely solid state – no moving parts
- Entirely bootable for current embedded O/S
- 50G operating shock
- 5G operating vibration
- 16.6 MB/s burst R/W rate
- 10 years data integrity



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Specifications:

Item	DDOM-SST-128M~256M	DDOM-SST-512G~4G		
IDE Transfer Mode	PIO Mode 0-4 MwDMA Mode 0-2	PIO Mode -6 MwDMA Mode 4 Ultra DMA Mode-4		
Drive Config.	Switch Master/Slave	Switch Master/Slave		
Protocol Mode	N/A	N/A		
Access Mode	N/A	N/A		
Data Transfer Rate		512M	1G	2G
Read Transfer Rate	>10Mbytes	>17Mbytes	>30MBytes	>30Mbytes
Write Transfer Rate	>5Mbytes	>5Mbytes	>10MBytes	>20MByte
Burst Transfer Rate	16.6MB/sec.			
Serials Physical				
Bus Interface	ATA Compatibility			
Connector	40/44pin IDE/ATA ANSI Standards			
Storage capacity	128M to 4GB			
Sector Size	512 bytes			
Driver Number	Drive 0 or 1			
Environmental Specification				
Operation Temp.	-45°C ~+85°C			
Storage Temp.	-65°C ~+150°C			
Humidity	10%~95% non-condensing			
Vibration	5G (7~2000Hz)			
Shock	50G/10ms			
System Reliability				
ECC technology	High Reliability based on the internal ECC function			
MTBF	>3,000,000 hours			
R/W Endurance	2,000,000 times (wear-leveling)			
Data integrity	10 years			
Power equirement				
DC input voltage	+5V single power supply operation			
Power mode	Auto Stand-by and sleep mode			
Power consumption	150mA (max.)			
Physical Specification				
Enclosure Materia	PC Mechanical Cover and UL-94			
Dimension	44 pin:48 x 32.6 mm (W x H)			



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C. Pin Assignments and Signal Descriptions

C.1 Pin Assignment

Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type
1	-RESET	I	2	GND	Ground
3	Data 7	I/O	4	Data 8	I/O
5	Data 6	I/O	6	Data 9	I/O
7	Data 5	I/O	8	Data 10	I/O
9	Data 4	I/O	10	Data 11	I/O
11	Data 3	I/O	12	Data 12	I/O
13	Data 2	I/O	14	Data 13	I/O
15	Data 1	I/O	16	Data 14	I/O
17	Data 0	I/O	18	Data 15	I/O
19	Ground	Power	20	Power Pin	Power
21	Reserved	--	22	GND	Ground
23	-IOW	I	24	GND	Ground
25	-IOR	I	26	GND	Ground
27	IORDY	O	28	Reserved	--
29	Reserved	--	30	GND	Ground
31	IRQ	O	32	-IOCS16	O
33	A1	I	34	-PDIAG	I/O
35	A0	I	36	A2	I
37	-CS0	I	38	-CSI	I
39	DASP	I/O	40	GND	Ground
41	VCC (Note1)	Power	42	VCC (Note1)	Power
43	GND (Note1)	Ground	44	Reserved (Note1)	--

Note 1 : These 4 pins are for IDE 44-pin standard.



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C.2 Signal Descriptions

Singal Name	Dir.	Pin	Description
RESET	I	1	This pin Host Reset. Reset signal is from the host and it is active low.
Data [15:0]	I/O	3-18	These lines carry Data, Command and Status information between the host and controller.D0 is LSB and D15 is MSB.
IOW	I	23	The I/O Write Storable pulse is used to clock I/O data on the Data bus into the controller registers. The clocking will occur on the negative to the positive edge of the signal (trailing edge).
IOR	I	25	This is an I/O Read strobe generated by the host. This signal gates I/O data into the bus from the controller. The clocking will occur on the negative to the positive edge of the signal (trailing edge).
IRQ	O	31	This is an interrupt request from the controller to host, asking for service. The output of this signal is tri-state when the interrupt are disabled by the host.
A[2:0]	I	33,35,36	A[2:0] are used to select the one of eight registers in the Task File.
CS0,CS	I	37,38	-CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
IORDY	O	27	This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.
IOCS16	O	32	This open drain output signal is asserted low by the controller to indicate to the host the current cycle is a 16-bit (word) data transfer.
PDIAG	I/O	34	This bi-directional open drain signal is asserted by the slave after an Execute Diagnostic command to indicate to the master it has passed it's diagnostics.
DASP	I/O	39	This open drain output is asserted low any time the drive is active. In a Master/Slave configuration, this signal is used the slave to inform the master which has slave present.
GND		02,19,22,24,26,30,40,43	Ground
VCC		20,41,42	+5V or 3.3V Power



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D. System Power Consumption

Dc Input Voltage (VCC)		3.3V / 5V \pm 5%
+5V Current (Average Value)	Maximum active mode:	80mA
	Maximum sleep mode:	150 μ A


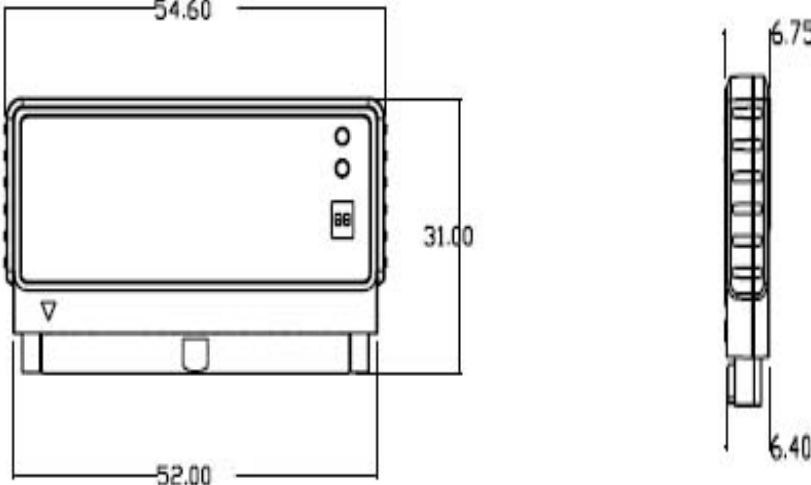


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E. Product Model and Physical Specification E1.44 Pin Vertical

Wide Temperature	-40°C ~ +85°C
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Model Name	DDOMSST-xxMB-44P-V
	
	



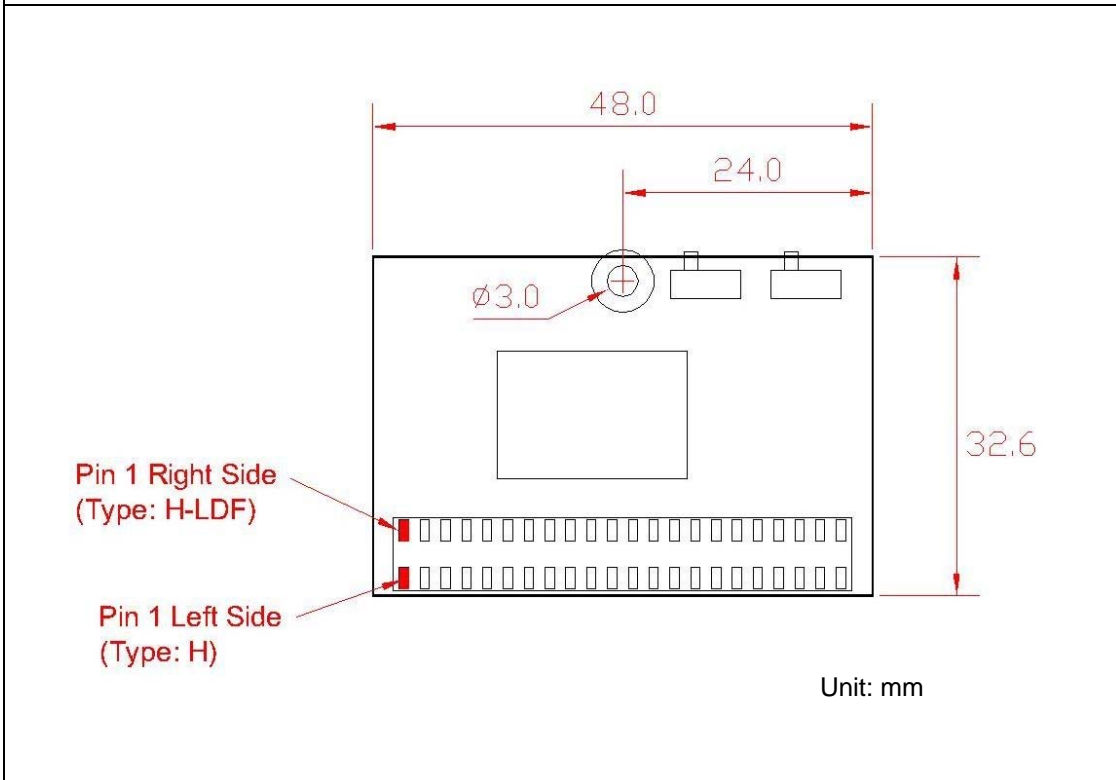
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E2.44 Pin Horizontal Left Side

Wide Temperature	-40°C ~ +85°C
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Model Name	DDOM-SST-xxMB-44P-HL
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E3.44 Pin Horizontal Right Side

Wide Temperature	-40°C ~ +85°C
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Model Name	DDOM-SST-xxMB-44P-H
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