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CT-CA56X

AMG G-Series G-T56N/G-T40E

COM Express™ Type 6 Module

User's Manual

Version 1.0

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http://www.candtsolution.com

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I. Preface

1.1 Disclaimer

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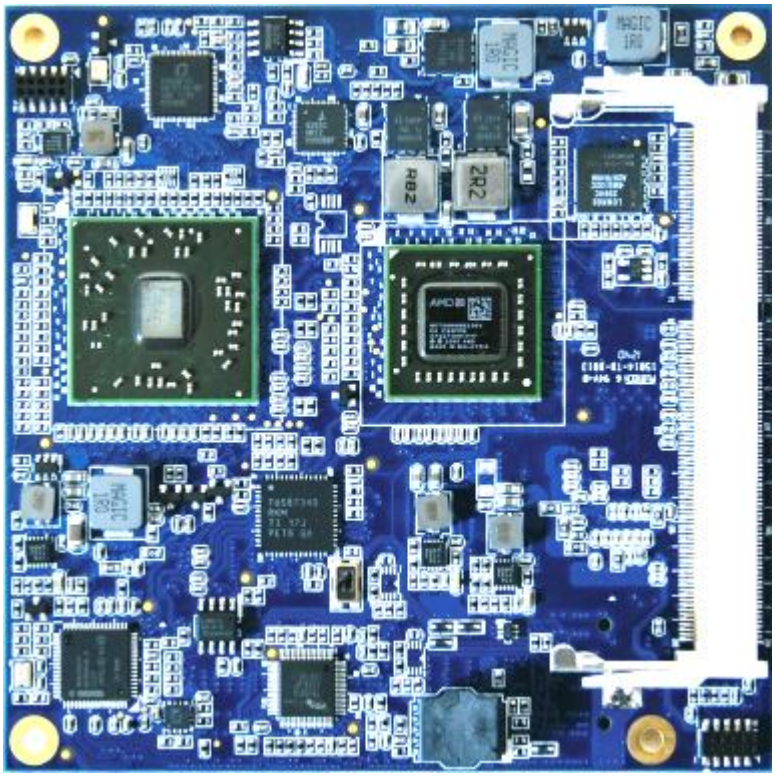
II. Introduction

2.1 Product Description



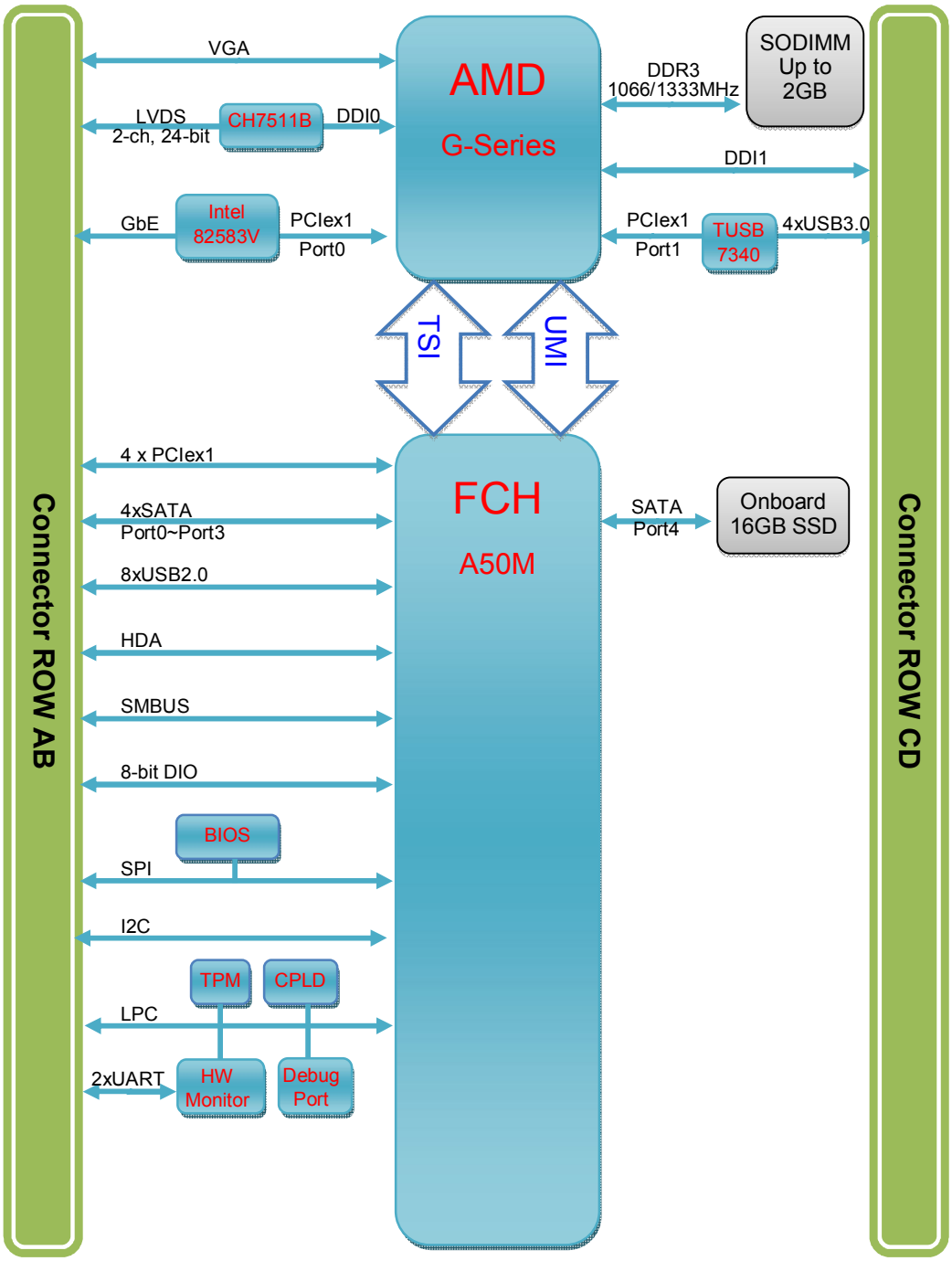
The CT-CA56X is a new COM (computer-on-module) Express® compact form factor (95x95mm) in embedded computing platforms. It combines the onboard AMD G-series processor with AMD FCH A50M chipset. The CT-CA56X is based on the COM Express® specification and features a standardized connector layout that carries a specified set of signals. With the Type 6 pin-out connectors, the CT-CA56X supports DDI/LVDS/VGA, SATA, HD audio, Gigabit Ethernet, PCIe and USB3.0. This system requires a Carrier Board to bring out I/O and power up. The benefit of this standardization pin-out is making the application design more flexible. To accommodate different ODM requirements, the COM Express module with a Carrier Board is the best cost-effective solution and reduces development time.

2.2 Specifications

- **CPU**
  - AMD G-T56N 1.65GHz Processor
  - AMD G-T40E 1.0GHz processor
- **Chipset**
  - AMD A50M FCH
- **System Memory**
  - One 204-pin DDR3 SODIMM socket
  - Data transfer rate:
    - 1066MHz for G-T40E
    - 1333MHz for G-T56N
  - Up to 4GB
- **BIOS**
  - AMI uEFI BIOS
  - 8MB SPI Flash ROM
- **SSD**
  - 16GB SSD onboard
- **TPM**
  - Trusted Platform Module compatible with TPM1.2
  - Infineon SLB9635
- **Graphics**
  - Dual display
  - CRT interface supports up to 2048x1536 MHz
  - Two channels of 24-bit LVDS interface supports resolution up to 1920x1200 MHz
  - One DDI port supports HDMI / DVI / DisplayPort / eDP
- **Ethernet**
  - Intel® 82583V GbE controller
  - One 10/100/1000 Base-Tx
- **Audio**
  - Integrated in chipset AMD A50M
- **SATA Interface**
  - Four SATA 3Gb/s ports
- **PCIe Lane**
  - Four PCIex1 Lane

- **USB Interface**
  - Eight USB 2.0 ports
  - Four USB 3.0 ports
- **LPC Interface**
- **SMBus**
- **SPI Interface**
- **8-bit GPIO**
- **Watchdog Timer**
- **H/W Monitor**
- **Power Management**
  - ACPI (Advanced Configuration and Power Interface)
- **Form Factor**
  - Compact size, 95mm x 95mm

2.3 Block Diagram



2.4 SKU

Product Number	Processor	PCH	Features
CT-CA561	AMD T-56N	A50M	1xDDR3, 24-bit LVDS, VGA, DDI, 4xPCIex1, GbE, 4xUSB3.0, 8xUSB2.0, 4xSATA, onboard 16GB SSD, TMP1.2
CT-CA562	AMD T-40E	A50M	1xDDR3, 24-bit LVDS, VGA, DDI, 4xPCIex1, GbE, 4xUSB3.0, 8xUSB2.0, 4xSATA, onboard 16GB SSD, TMP1.2
CT-CA563	AMD T-40E	A50M	1xDDR3, 24-bit LVDS, VGA, DDI, 4xPCIex1, GbE, 4xUSB3.0, 8xUSB2.0, 4xSATA, TMP1.2

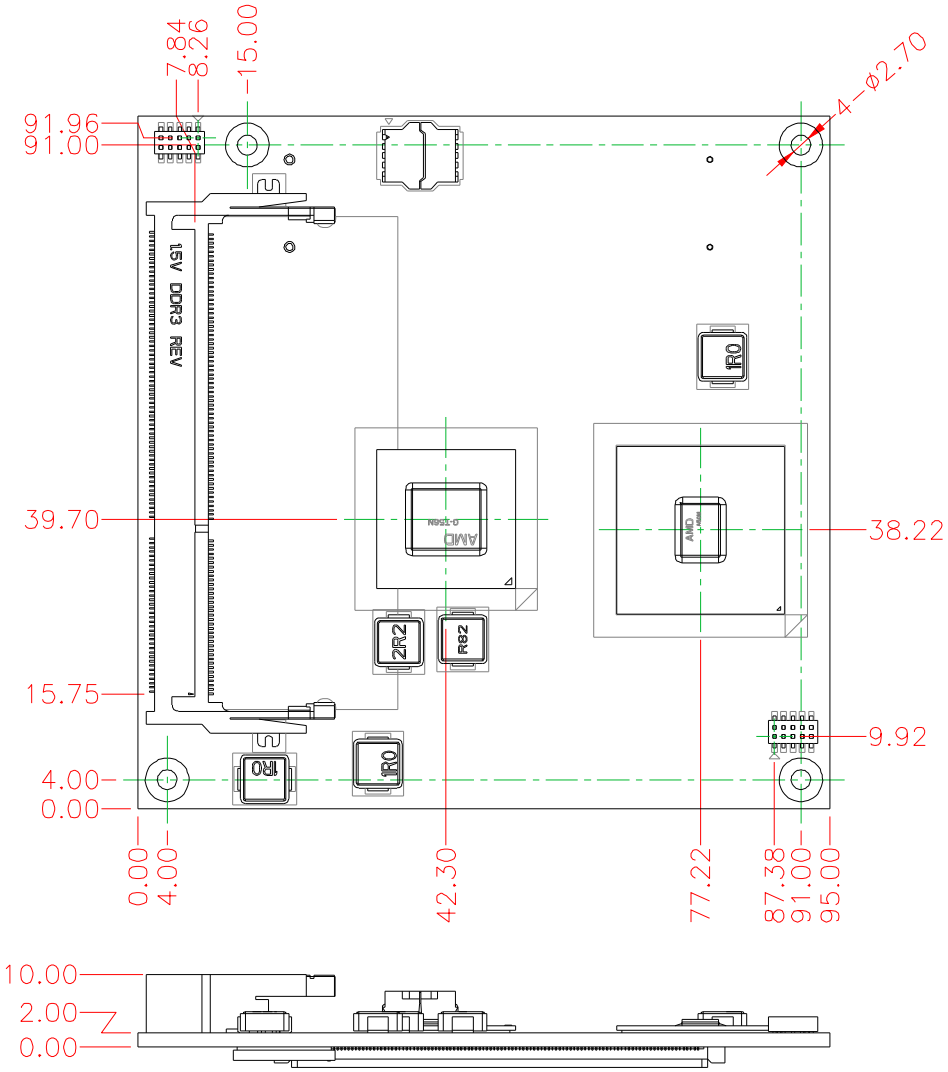
III. Mechanical Specification

3.1 Module Dimensions

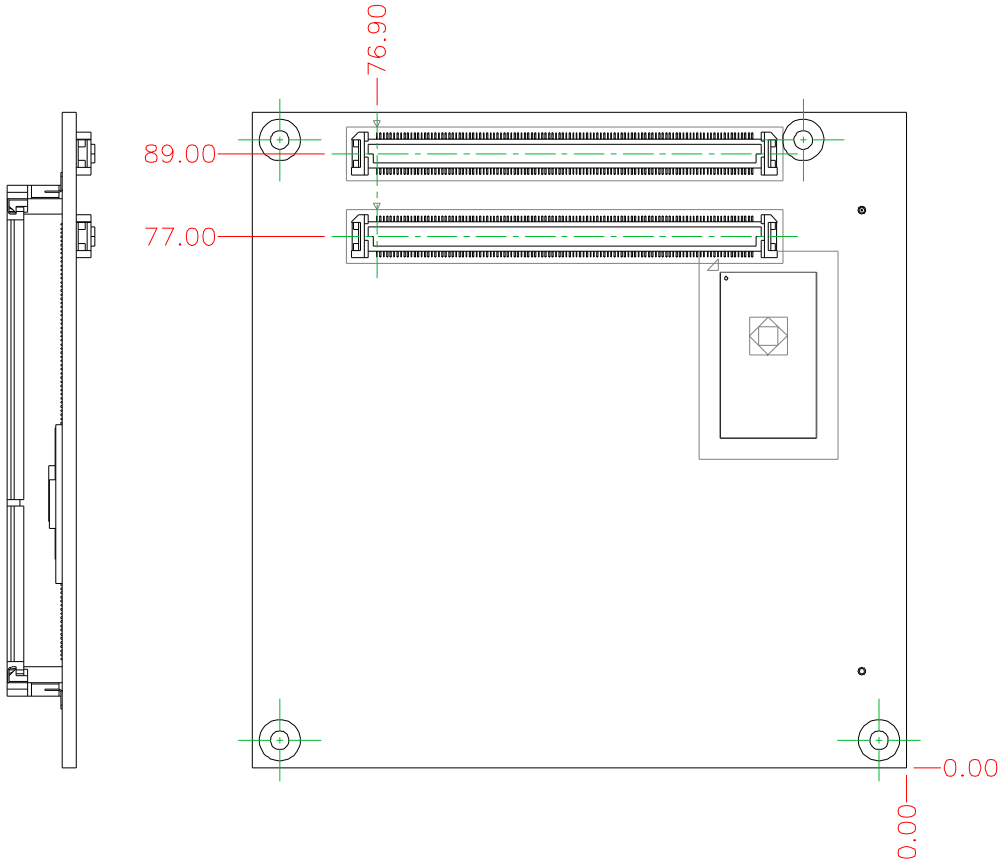
The PCB size of CT-CA56X is 95mm x 95mm, the standard COM Express compact Module size.

The holes shown in the drawing below is for stacking the module with the Heat Spreader / Heat Sink and the Carrier Board. The mounting holes are 2.7mm, and the 2.5mm hardware shall be used. The position and the dimension of the holes are shown in the unit of millimeters.

Top View:



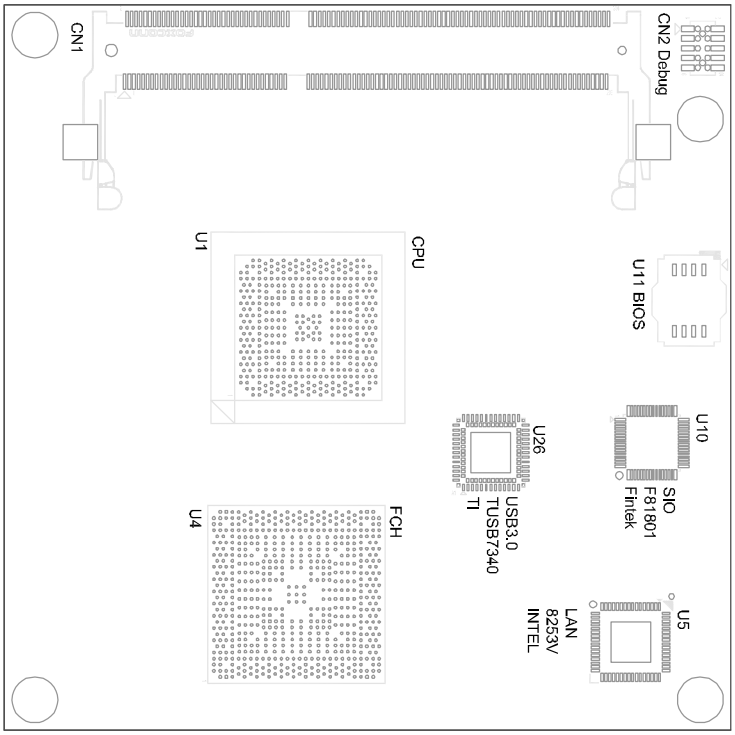
Side View and Bottom View:



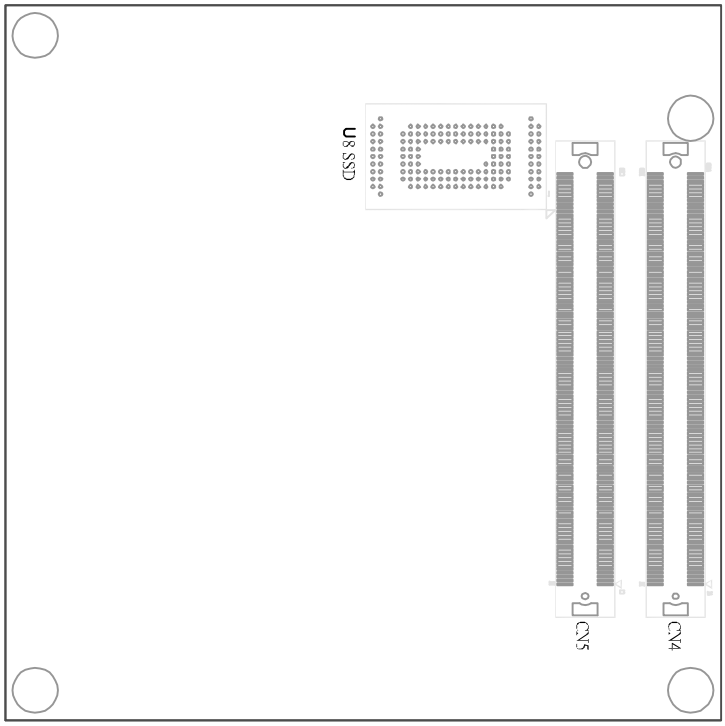
3.2 Layout

There is one SODIMM socket mounted on the top side of the CT-CA56X. Two 220-pin COM Express connectors are mounted at the bottom side of the PCB.

Top View:



Bottom View:



3.3 Connectors

Connector	Description
CN1	SODIMM Socket
CN2	LPC Debug Port
CN3	CPLD JTAGE
CN4	COM™ Express connector Row A, B
CN5	COM™ Express connector Row C, D

3.3.1 LPC Debug Port: CN2

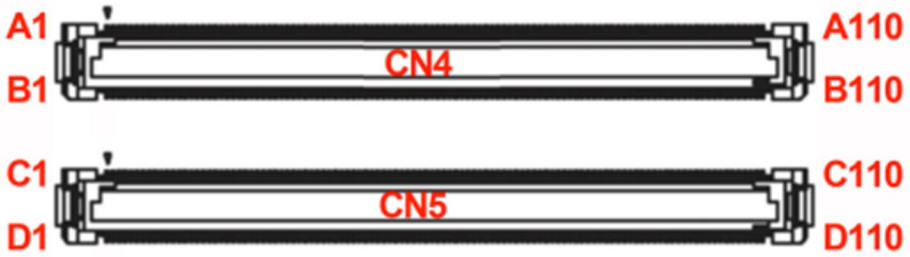
Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	LPC_AD3	4	BIOS_DIS0-L
5	LPC_AD2	6	RESET
7	LPC_AD1	8	CLOCK
9	LPC_AD0	10	FRAME

3.3.2 CPLD JTAGE: CN3

Pin	Signal	Pin	Signal
1	+3.3V	2	GND
3	TDO	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND

3.3.3 COM Express Connectors

The CT-CA56X is connected to the carrier board via two 220-pin connectors. Each connector is break down into two rows. The first connector, CN4, consists Row A and Row B; the second connector, CN5, consists Row C and Row D. Their pin-outs are as table below.



Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GND	GND
3	GBE0_MDI3+	LPC_FRAME#	USB_SSRX0-	USB_SSTX0-
4	GBE0_LINK100#	LPC_AD0	USB_SSRX0+	USB_SSTX0+
5	GBE0_LINK1000#	LPC_AD1	GND	GND
6	GBE0_MDI2-	LPC_AD2	USB_SSRX1-	USB_SSTX1-
7	GBE0_MDI2+	LPC_AD3	USB_SSRX1+	USB_SSTX1+
8	GBE0_LINK#	LPC_DRQ0#	GND	GND
9	GBE0_MDI1-	LPC_DRQ1#	USB_SSRX2-	USB_SSTX2-
10	GBE0_MDI1+	LPC_CLK	USB_SSRX2+	USB_SSTX2+
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#-	USB_SSRX3-	USB_SSTX3-
13	GBE0_MDI0+	SMB_CK	USB_SSRX3+	USB_SSTX3+
14	GBE0_CTREF	SMB_DAT	GND	GND
15	SUS_S3#	SMB_ALERT#	DDI1_PAIR6+	DDI1_CTRLCLK_AUX+
16	SATA0_TX+	SATA1_TX+	DDI1_PAIR6-	DDI1_CTRLDATA_AUX-
17	SATA0_TX-	SATA1_TX-	RSVD	RSVD
18	SUS_S4#	SUS_STAT#	RSVD	RSVD
19	SATA0_RX+	SATA1_RX+	PCIE_RX6+	PCIE_TX6+
20	SATA0_RX-	SATA1_RX-	PCIE_RX6-	PCIE_TX6-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	PCIE_RX7+	PCIE_TX7+
23	SATA2_TX-	SATA3_TX-	PCIE_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	DDI1_HPD	RSVD
25	SATA2_RX+	SATA3_RX+	DDI1_PAIR4+	RSVD
26	SATA2_RX-	SATA3_RX-	DDI1_PAIR4-	DDI1_PAIR0+
27	BATLOW#	WDT	RSVD	DDI1_PAIR0-
28	(S)ATA_ACT#	AC/HAD_SDIN2	RSVD	RSVD
29	AC/HDA_SYNC	AC/HAD_SDIN1	DDI1_PAIR5+	DDI1_PAIR1+
30	AC/HAD_RST#	AC/HAD_SDIN0	DDI1_PAIR5-	DDI1_PAIR1-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR	DDI2_CTRLCLK_AUX+	DDI1_PAIR2+
33	AC/HAD_SDOUT	I2C_CK	DDI2_CTRLDATA_AUX-	DDI1_PAIR2-
34	BIOS_DIS0#	I2C_DAT	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL
35	THRMTRIP#	THRM#	RSVD	RSVD
36	USB6-	USB7-	DDI3_CTRLCLK_AUX+	DDI1_PAIR3+
37	USB6+	USB7+	DDI3_CTRLDATA_AUX-	DDI1_PAIR3-
38	USB_6_7_OC#	USB_4_5_OC#	DDI3_DDC_AUX_SEL	RSVD

Pin	Row A	Row B	Row C	Row D
39	USB4-	USB5-	DDI3_PAIR0+	DDI2_PAIR0+
40	USB4+	USB5+	DDI3_PAIR0-	DDI2_PAIR0-
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	DDI3_PAIR1+	DDI2_PAIR1+
43	USB2+	USB3+	DDI3_PAIR1-	DDI2_PAIR1-
44	USB_2_3_OC#	USB_0_1_OC#	DDI3_HPD	DDI2_HPD
45	USB0-	USB1-	RSVD	RSVD
46	USB0+	USB1+	DDI3_PAIR2+	DDI2_PAIR2+
47	VCC_RTC	EXCD1_PERST#	DDI3_PAIR2-	DDI2_PAIR2-
48	EXCD0_PERST#	EXCD1_CPPE#	RSVD	RSVD
49	EXCD0_CPPE#	SYS_RESET#	DDI3_PAIR3+	DDI2_PAIR3+
50	LPC_SERIRQ	CB_RESET#	DDI3_PAIR3-	DDI2_PAIR3-
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PEG_RX0+	PEG_TX0+
53	PCIE_TX5-	PCIE_RX5-	PEG_RX0-	PEG_TX0-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PEG_RX1+	PEG_TX1+
56	PCIE_TX4-	PCIE_RX4-	PEG_RX1-	PEG_TX1-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PEG_RX2+	PEG_TX2+
59	PCIE_TX3-	PCIE_RX3-	PEG_RX2-	PEG_TX2-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PEG_RX3+	PEG_TX3+
62	PCIE_TX2-	PCIE_RX2-	PEG_RX3-	PEG_TX3-
63	GPI1	GPO3	RSVD	RSVD
64	PCIE_TX1+	PCIE_RX1+	RSVD	RSVD
65	PCIE_TX1-	PCIE_RX1-	PEG_RX4+	PEG_TX4+
66	GND	WAKE0#	PEG_RX4-	PEG_TX4-
67	GPI2	WAKE1#	RSVD	GND
68	PCIE_TX0+	PCIE_RX0+	PEG_RX5+	PEG_TX5+
69	PCIE_TX0-	PCIE_RX0-	PEG_RX5-	PEG_TX5-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	PEG_RX6+	PEG_TX6+
72	LVDS_A0-	LVDS_B0-	PEG_RX6-	PEG_TX6-
73	LVDS_A1+	LVDS_B1+	GND	GND
74	LVDS_A1-	LVDS_B1-	PEG_RX7+	PEG_TX7+
75	LVDS_A2+	LVDS_B2+	PEG_RX7-	PEG_TX7-
76	LVDS_A2-	LVDS_B2-	GND	GND

Pin	Row A	Row B	Row C	Row D
77	LVDS_VDD_EN	LVDS_B3+	RSVD	RSVD
78	LVDS_A3+	LVDS_B3-	PEG_RX8+	PEG_TX8+
79	LVDS_A3-	LVDS_BKLT_EN	PEG_RX8-	PEG_TX8-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	PEG_RX9+	PEG_TX9+
82	LVDS_A_CK-	LVDS_B_CK-	PEG_RX9-	PEG_TX9-
83	LVDS_I2C_CK	LVDS_BKLT_CTR	RSVD	RSVD
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PEG_RX10+	PEG_TX10+
86	RSVD	VCC_5V_SBY	PEG_RX10-	PEG_TX10-
87	RSVD	VCC_5V_SBY	GND	GND
88	PCIE_CK_REF+	BIOS_DIS1#	PEG_RX11+	PEG_TX11+
89	PCIE_CK_REF-	VGA_RED	PEG_RX11-	PEG_TX11-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN	PEG_RX12+	PEG_TX12+
92	SPI_MISO	VGA_BLU	PEG_RX12-	PEG_TX12-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PEG_RX13+	PEG_TX13+
95	SPI_MOSI	VGA_I2C_CK	PEG_RX13-	PEG_TX13-
96	TPM_PP	VGA_I2C_DAT	GND	GND
97	TYPE10#	SPI_CS#	RSVD	RSVD
98	SER0_TX	RSVD	PEG_RX14+	PEG_TX14+
99	SER0_RX	RSVD	PEG_RX14-	PEG_TX14-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	SER1_TX	FAN_PWMOUT	PEG_RX15+	PEG_TX15+
102	SER1_RX	FAN_TACHIN	PEG_RX15-	PEG_TX15-
103	LID#	SLEEP#	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

3.4 Thermal Solutions

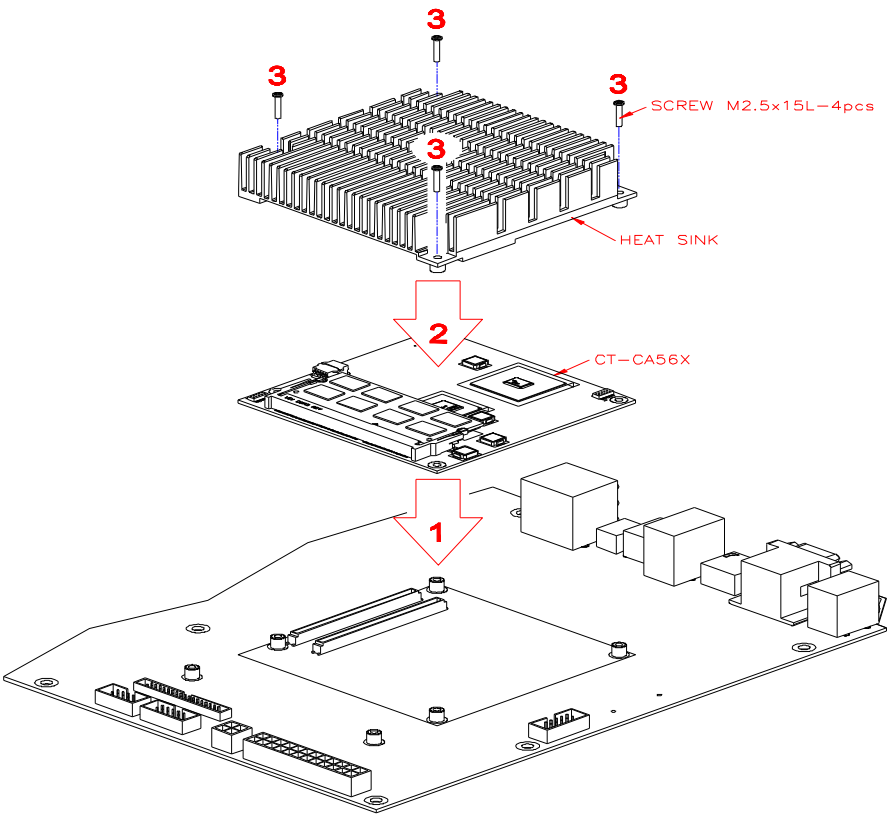
There are three thermal solutions for the COM Express Module CT-CA56X to dissipate the heat. A heat sink, a fan sink or a heat spreader can be used, and to assemble any of them with CT-CA56X module and a Carrier Board is the same.

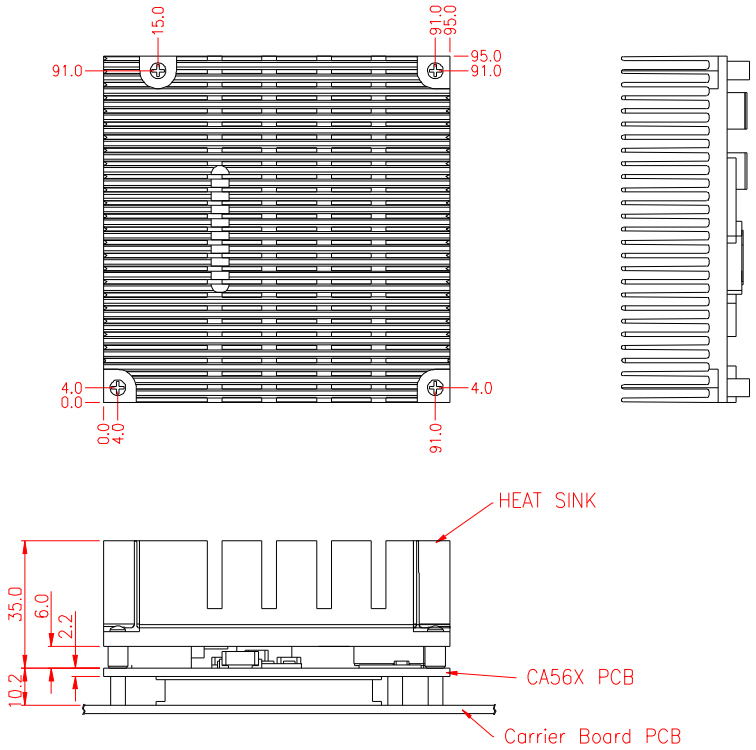
3.4.1 Heat Sink

Step 1: Connect the COM Express connectors on the module, CT-CA56X, to the corresponding COM connectors on the Carrier Board. Make sure the four holes at the corners of CT-CA56X module align to the corresponding pillars on the Carrier Board.

Step2: Place the heat sink on top of the CT-CA56X module.

Step3: Use four screws (M2.5x15L) to secure the heat sink with the Carrier Board through the corresponding holes on the CT-CA56X.



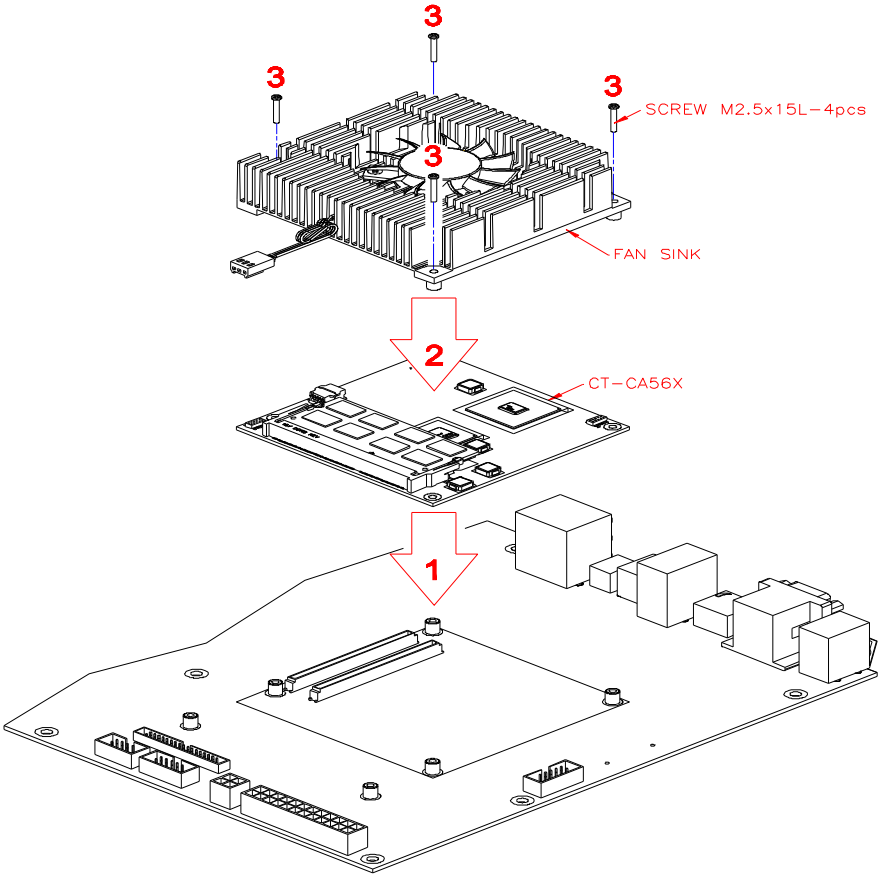


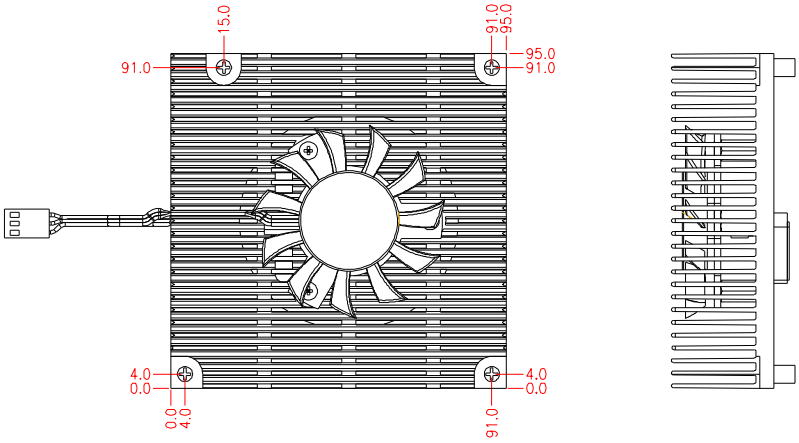
3.4.2 Fan Sink

Step 1: Connect the COM Express connectors on the module, CT-CA56X, to the corresponding COM connectors on the Carrier Board. Make sure the four holes at the corners of CT-CA56X module align to the corresponding pillars on the Carrier Board.

Step2: Place the fan sink on top of the CT-CA56X module.

Step3: Use four screws (M2.5x15L) to secure the fan sink with the Carrier Board through the corresponding holes on the CT-CA56X.


3
3
3
3
SCREW M2.5x15L-4pcs
FAN SINK
2
CT-CA56X
1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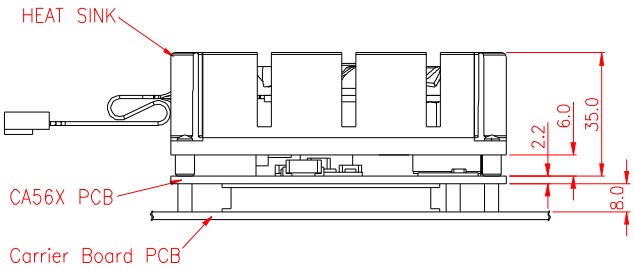

HEAT SINK
CA56X PCB
Carrier Board PCB
2.2
6.0
35.0
8.0

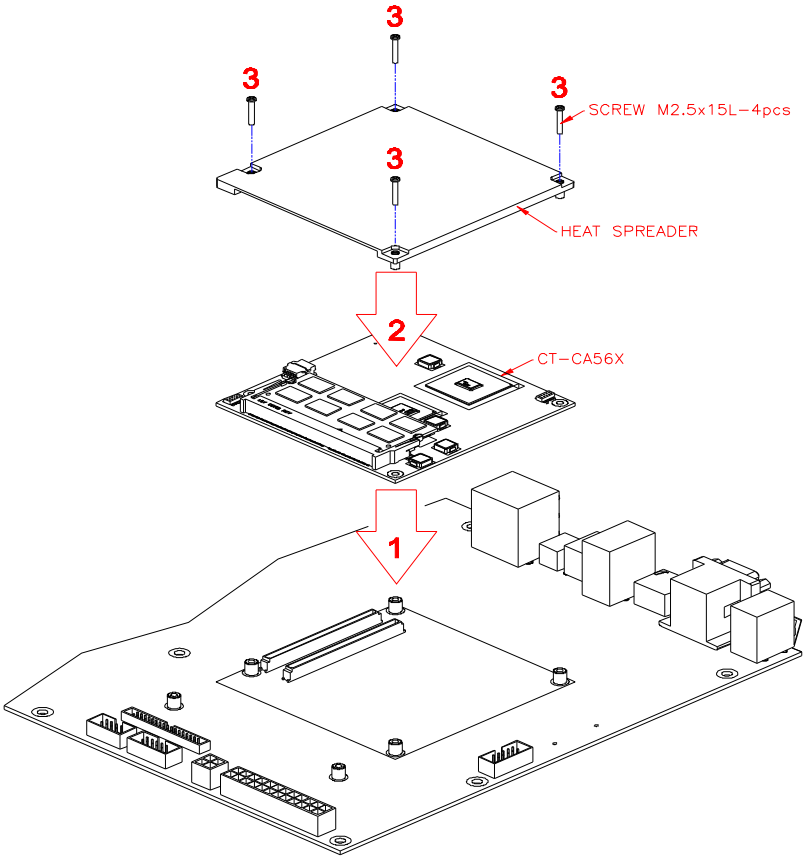
3.4.3 Heat Spreader

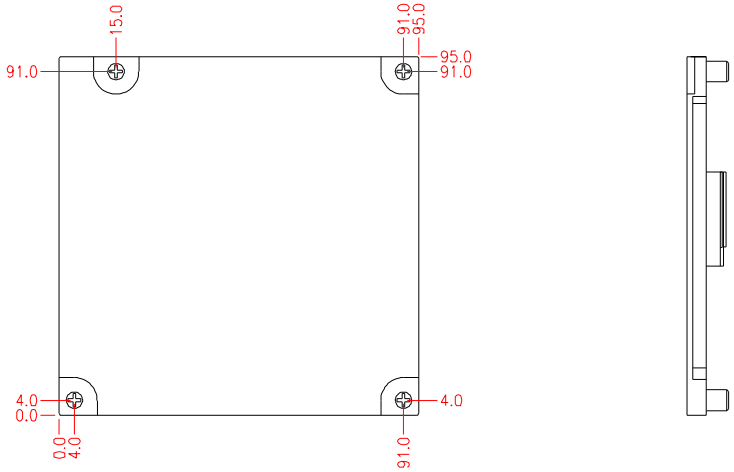
A heat spreader is designed for the CT-CA56X to dissipate heat. All heat generating components are thermally conducted to the heat spreader in order to avoid hot spots.

Step 1: Connect the COM Express connectors on the module, CT-CA56X, to the corresponding COM connectors on the Carrier Board. Make sure the four holes at the corners of CT-CA56X module align to the corresponding pillars on the Carrier Board.

Step2: Place the heat spreader on top of the CT-CA56X module.

Step3: Use four screws (M2.5x15L) to secure the heat sink with the Carrier Board through the corresponding holes on the CT-CA56X.

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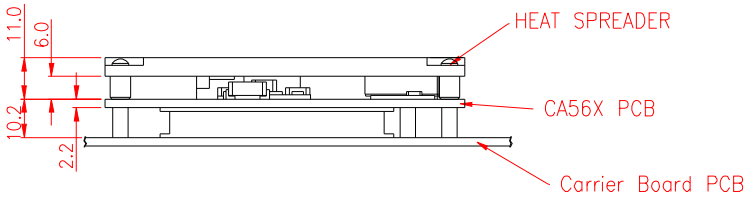

11.0
6.0
10.2
2.2
HEAT SPREADER
CA56X PCB
Carrier Board PCB

IV. Features & Interfaces

4.1 Processor

The CT-CA56X supports compact BGA AMD G-Series T-56N or T-40E Accelerated Processing Unit. This AMD Embedded G-Series APU integrates a low power processor and advanced GPU to deliver high performance multi-media content in a small and power efficient form factor.

4.2 BIOS

The AMI uEFI BIOS, 8MB SPI Flash ROM is used in the CT-CA56X module.

4.3 System Memory

The Integrated Memory Controller (IMC) of the processor supports one 64-bit channel of DDR3 protocols. The channel with a 204-pin SODIMM socket allows the data transfer rate of 1333MHz for G-T56N and 1066MHz for G-T40E. The maximum size of the Memory is 4GB.

4.4 Graphics

The AMD G-T56N APU contains an AMD Radeon HD6320 graphics unit, and the AMD G-T40E APU contains an AMD Radeon HD6250. Each APU supports single or dual-independent high-resolution display. The graphic core frequency is 500 MHz at G-T56N and 280 MHz at G-T40E.

4.4.1 Analog Display Port

The Analog Port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated Display Data Channel (DDC) signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT Based monitor with a VGA connector. The Analog Port can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 60Hz.

Signal	I/O	Description
VGA_RED	O	Red for monitor, analog DAC output, designed to drive a 37.5Ω equivalent load.
VGA_GRN	O	Green for monitor, analog DAC output, designed to drive a 37.5Ω equivalent load.
VGA_BLU	O	Blue for monitor, analog DAC output, designed to drive a 37.5Ω equivalent load.
VGA_HSYNC	O	Horizontal sync output to VGA monitor
VGA_VSYNC	O	Vertical sync output to VGA monitor
VGA_I2C_CLK	I/O	Monitor clock line
VGA_I2C_DATA	I/O	Monitor data line

4.4.2 LVDS

Each of the two LVDS transmitter channel consists of 4 data pairs and a clock pair. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals. The maximum resolution is 1920x1200.

Signal	I/O	Description
LVDS_A/B[3:0]+	O	Differential data output
LVDS_A/B[3:0]-	O	Differential data output
LVDS_A/B_CLK+	O	Differential clock output - positive
LVDS_A/B_CLK-	O	Differential clock output - negative
LVDS_VDD_EN	O	LVDS panel power enable
LVDS_BKLT_EN	O	Panel backlight enable control
LVDS_BKLT_CTR	O	Panel backlight brightness control
LVDS_I2C_CLK	I/O	LVDS flat panel I2C clock for EDID read and control.
LVDS_I2C_DATA	I/O	LVDS flat panel I2C data for EDID read and control.

4.4.3 Digital Display Interfaces (DDI)

The graphic control of AMD G-Series APU can drive HDMI, DVI, eDP and Display Port natively. Its two display ports can support up to two different images on two different display devices.

Signal	I/O	Description
DDI[1:2]_PAIR[0:3]+ DDI[1:2]_PAIR[0:3]-	O	DDI 1 and 2 Pair[0:3] differential pairs
DDI[1:2]_DDC_AUX_SEL	I	Selects the function of DDI[1:2]_CTRLCLK_AUX+ and DDI[1:2]_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CTRLCLK and CTRLDATA signals.
DDI[1:2]_CTRLCLK_AUX+	I/O	DP AUX+ function if DDI[1:2]_DDC_AUX_SEL is no connect
	I/O	HDMI/DVI I2C CTRLCLK if DDI[1:2]_DDC_AUX_SEL is pulled high
DDI[1:2]_CTRLDATA_AUX-	I/O	DP AUX- function if DDI[1:2]_DDC_AUX_SEL is no connect
	I/O	HDMI/DVI I2C CTRLDATA if DDI[1:2]_DDC_AUX_SEL is pulled high
DDI[1:2]_HPD	I	DDI Hot-Plug Detect

	Signal	Pin	eDP/DP	HDMI/DVI
DDI 1	DDI1_PAIR0+	D26	DP1_LANE0+	TMDS1_DATA2+
	DDI1_PAIR0-	D27	DP1_LANE0-	TMDS1_DATA2-
	DDI1_PAIR1+	D29	DP1_LANE1+	TMDS1_DATA1+
	DDI1_PAIR1-	D30	DP1_LANE1-	TMDS1_DATA1-
	DDI1_PAIR2+	D32	DP1_LANE2+	TMDS1_DATA0+
	DDI1_PAIR2-	D33	DP1_LANE2-	TMDS1_DATA0-
	DDI1_PAIR3+	D36	DP1_LANE3+	TMDS1_CLK+
	DDI1_PAIR3-	D37	DP1_LANE3-	TMDS1_CLK-
	DDI1_CTRLCLK_AUX+	D15	DP1_AUX+	TMDS1_SCL
	DDI1_CTRLDATA_AUX-	D16	DP1_AUX-	TMDS1_SDA
	DDI1_DDC_AUX_SEL	D34	CONFIG1 (pull down to GND)	Pull up to 5V
	DDI1_HPD (3.3V active high signal)	C24		
	Signal	**Pin**	**DP**	**HDMI/DVI**
DDI 2	DDI2_PAIR0+	D39	DP2_LANE0+	TMDS2_DATA2+
	DDI2_PAIR0-	D40	DP2_LANE0-	TMDS2_DATA2-
	DDI2_PAIR1+	D42	DP2_LANE1+	TMDS2_DATA1+
	DDI2_PAIR1-	D43	DP2_LANE1-	TMDS2_DATA1-
	DDI2_PAIR2+	D46	DP2_LANE2+	TMDS2_DATA0+
	DDI2_PAIR2-	D47	DP2_LANE2-	TMDS2_DATA0-

	DDI2_PAIR3+	D49	DP2_LANE3+	TMDS2_CLK+
	DDI2_PAIR3-	D50	DP2_LANE3-	TMDS2_CLK-
	DDI2_CTRLCLK_AUX+	C32	DP2_AUX+	HDMI2_SCL
	DDI2_CTRLDATA_AUX-	C33	DP2_AUX-	HDMI2_SDA
	DDI2_DDC_AUX_SEL	C34	CONFIG1 (pull down to GND)	Pull up to 5V
	DDI2_HPD (3.3V active high signal)	D44		

4.4.3.1 High Definition Multimedia Interface (HDMI)

The HDMI is provided for transmitting uncompressed digital audio and video signals to television sets, projectors and other video displays.

4.4.3.2 Digital Video Interface (DVI)

The PCH digital ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver, which is similar to the HDMI protocol but the audio and CEC. When a system has support for DVI-I port, then either VGA or the DVI-D through a single DVI-I connector can be driven but not both simultaneously.

The HDMI or DVI supports the resolution up to 1920x1200 at 60Hz.

HDMI Signal	I/O	Description
TMDS[1:2]_CLK+ TMDS[1:2]_CLK-	O	HDMI/DVI TMDS Clock differential pair
TMDS[1:2]_DATA[0:2]+ TMDS[1:2]_DATA[0:2]-	O	HDMI/DVI TMDS lanes 0, 1 and 2 differential pairs
HDMI[1:2]_SCL	I/O	HDMI/DVI I2C control clock
HDMI[1:2]_SDA	I/O	HDMI/DVI I2C control data

4.4.3.3 Display Port (DP)

The Display Port is a digital communication interface that utilized differential signaling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. The Display Port supports the resolution up to 2560x1600.

4.4.3.4 Embedded DisplayPort (eDP)

Embedded DisplayPort (eDP) is an embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. eDP is supported only on Digital Display Port 1. The resolution is up to 2560x1600.

DP Signal	I/O	Description
DP[1:2]_LANE[0:3]+ DP[1:2]_LANE[0:3]-	O	Uni-directional main link for the transport of isochronous streams and secondary-data packets
DP[1:2]_AUX+ DP[1:2]_AUX-	I/O	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access

4.5 Chipset

The Fusion Controller Hub (FCH) used on CT-CA56X is AMD A50M. The FCH provides extensive I/O support with two COM™ Express connectors.

4.6 USB

4.6.1 USB 2.0

The four OHCI and three EHCI host Controllers of AMD® A50M offer eight USB2.0 ports. Each USB2.0 port supports USB 1.1 and 2.0 compliant devices.

Signal	I/O	Description
USB[0:7]+ USB[0:7]-	I/O	USB differential pairs, channels 0 through 7
USB_0_1_OC#	I	USB over-current sense, USB 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	I	USB over-current sense, USB 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	I	USB over-current sense, USB 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.

Signal	I/O	Description
USB_6_7_OC#	I	USB over-current sense, USB 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.

4.6.1 USB 3.0

There are four USB 3.0 ports by extended from the Port 1 of the PCIe x1 interface in AMD G-series APU.

Signal	I/O	Description
USB_SSRX[0:3]+ USB_SSRX[0:3]-	I	USB differential pairs, channels 0 through 3, receive Data/Address/Command signals
USB_SSTX[0:3]+ USB_SSTX[0:3]-	I	USB differential pairs, channels 0 through 3, transmit Data/Address/Command signals

4.7 SATA

The FCH A50M provides five independent Serial ATA (SATA) channels. Four Channels supports Port 0 and 3 for general SATA devices with 3.0 Gb/s transfer rate. The other channel is for Port 4, is used for onboard 16GB SSD.

Signal	I/O	Description
SATA[0..3]_TX+ SATA[0..3]_TX-	O	Serial ATA Port 0~3 transmit differential pair
SATA[0..3]_RX+ SATA[0..3]_RX-	I	Serial ATA Port 0~3 receive differential pair
(S)ATA_ACT#	OC	ATA (parallel and serial) activity indicator, active low

4.8 PCI Express

4.8.1 PCI Express x1

There are four one-lane PCI Express ports available in the FCH A50M. The ports are compliant to the PCI Express 1.0 specification running at 2.5 Gb/s.

Signal	I/O	Description
PCIE[2:5]_TX+ PCIE[2:5]_TX-	O	PCI Express Differential transmit Pairs 2 through 5
PCIE[2:5]_RX+ PCIE[2:5]_RX-	I	PCI Express Differential receive Pairs 2 through 5
PCIE_CK_REF0+ PCIE_CK_REF0-	O	Reference clock output for all PCI Express and PCI Express Graphics lanes

4.9 High Definition Audio

The High Definition Audio (HDA) controller is integrated with FCH A50M. It communicates with the external codec(s) over the High Definition Audio link. The Hudson-M1 HD Audio Controller consists of four independent output DMA engines and four independent input DMA engines that are used to move data between system memory and an external codec(s). The FCH implements a single Serial Data Output signal (HDA_SDOUT) that is connected to all external codecs. Three Serial Digital Input signals (HDA_SDIN[2:0]) provided by the FCH support up to three codecs.

Signal	I/O	Description
AC/HDA_RST#	O	Reset output to CODEC, active low
AC/HDA_SYNC	O	Sample-synchronization signal to the CODEC(s)
AC/HDA_BITCLK	O	Serial data clock generated by the external CODEC(s)
AC/HDA_SDOUT	O	Serial TDM data output to the CODEC
AC/HDA_SDIN[2:0]	I/O	Serial TDM data input from up to 3 CODECs

4.10 Ethernet

The Intel® 82583V, a fully-integrated Gigabit Ethernet Media Access Control (MAC) provides 10/100/1000Mb/s Ethernet interface. The Intel® 82583V is connected to Port 0 of the PCIe x1 in the AMD G-series APU. Gigabit transformer has to be designed on the Carrier Board.
The integrated GbE controller contains power management registers for PCIE, so it supports the Advanced Configuration and Power Interface (ACPI) specification. This enables the network-related activity (using an internal host wake signal) to wake up the host.

Signal	I/O	Description
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	I/O	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100 and 10 Mbit/sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- / B1_DA+/- / TX+/- / TX+/- MDI[1]+/- / B1_DB+/- / RX+/- / RX+/- MDI[2]+/- / B1_DC+/- MDI[3]+/- / B1_DD+/-
GBE0_ACT#	OD	Gigabit Ethernet Controller 0 activity indicator, active low
GBE0_LINK#	OD	Gigabit Ethernet Controller 0 link indicator, active low
GBE0_LINK100#	OD	Gigabit Ethernet Controller 0 100 Mbit/sec link indicator, active low
GBE0_LINK1000#	OD	Gigabit Ethernet Controller 0 1000 Mbit/sec link indicator, active low
GBE0_CTREF	REF	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is 3.3V.

4.11 LPC

The LPC interface provides legacy I/O support on a Carrier Board via a Super I/O and system management devices.

Signal	I/O	Description
LPC_AD[3:0]	I/O	LPC multiplexed address, command and data
LPC_FRAME#	O	LPC frame indicates the start of an LPC cycle
LPC_DRQ[0:1]#	I	LPC serial DMA request input

Signal	I/O	Description
LPC_SERIRQ	I/O	LPC serial interrupt
LPC_CLK	O	LPC clock output – 33MHz nominal

4.12 SPI

The Serial Peripheral Interface (SPI) is a 4-pin interface that supports SPI-compatible flash devices. The SPI flash device can be up to 16MB (128Mb). The SPI bus is clocked at either 20MHz, 25MHz, 33MHz or 50 MHz. SPI devices selected should support one of these frequencies.

Signal	I/O	Description
SPI_CS#	O	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1
SPC_MISO	I	Data in to Module from Carrier SPI
SPI_MISI	O	Data out from Module to Carrier SPI
SPI_CLK	O	Clock from Module to Carrier SPI
SPI_POWER	O	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100ma of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board.

4.13 UART

The CT-CA56X module supports two serial RX/TX ports.

Signal	I/O	Description
SER[0:1]_TX	O	UART transmitter
SER[0:1]_RX	I	UART receiver

4.14 SMBus

The SMBus port is specified for system management functions. It is used on the Module to manage system function such as reading the DRAM SPD EEPROM and setting clock synthesizer parameters. If the SMBus is used on the carrier board, then great care must be taken that no conflicts with the on-Module SMBus devices occur. It may be useful for implementation on the

Carrier Board of standards such as Smart Battery. The maximum capacitance on the Carrier Board shall not exceed 100pF.

Signal	I/O	Description
SMB_CK	I/OD	System Management Bus bidirectional clock line
SMB_DAT	I/OD	System Management Bus bidirectional data line
SMB_ALERT#	I	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

4.15 ExpressCard

ExpressCard is a small form factor expansion card that uses PCI Express or USB as the interface. It is similar in concept and scope to CardBus. The CT-CA56X supports two Express Card interface.

Signal	I/O	Description
EXCD[0:1]_CPPE#	I	PCI ExpressCard: PCI Express capable card request, active low, one per card
EXCD[0:1]_PERST#	O	PCI ExpressCard: reset, active low, one per card

4.16 General Purpose Input Output

GPI and GPO pins may be implemented as GPIO (Module specific). GPI and GPO pins may be implemented as SDIO.

Signal	I/O	Description
GPO[0:3]	O	General purpose output pins. Upon a hardware reset, these outputs should be low
GPI[0:3]	I	General purpose input pins. Pulled high internally on the Module.

4.16.1 GPIO Configuration

Output Pin default setting is HIGH.

Pin #	GPIO#	Default Configuration
C22	GPIO224	**GPO3**
A23	GPIO222	**GPO2**
C24	GPIO220	**GPO1**

Pin #	GPIO#	Default Configuration
D24	GPIO218	**GPO0**
A24	GPIO215	**GPI3**
A26	GPIO213	**GPI2**
B27	GPIO211	**GPI1**
B28	GPIO209	**GPI0**

The GPIO function, provided by AMD A50M, can be accessed through GPIO Base Address Register (GPIOBASE). This address is at memory-mapped IOs. The configuration on CT-CA56X is described as below.

Register	Address
GPIOBASE Base Address	0xFED80100

The memory I/O read/write function is used to access and configure the AMD A50M. Through the memory I/O read or write command, the current status of GPIO can configure each pin to input or output.

4.16.2 Registers Description

4.16.2.1 GPIO Use Select Register

Gpio<N> – R/W 8 bits - [Gpio_Reg: NNh]			
Field Name	**Bits**	**Default**	**Description**
OwnedBylmc	0	0	This bit can only be written by IMC. If this bit is set, only IMC can write to bits 6:2 and bit 1 can no longer be written by host. This bit is always sticky.
OwnedByHost	1	0	This bit can only be written by host (BIOS). If this bit is set, only host can write to bits 6:2 and bit 0 can no longer be written by IMC. This bit is always sticky.
Sticky	2	0	If set, bits 6:3 are sticky. If cleared, bits 6:3 are reset back to default values whenever a reset occurs. This will allow every GPIO to be sticky or non-sticky
PullUpB	3	0	0: Pull-up enable 1: Pull-up disabled
PullDown	4	0	0: Pull down disabled 1: Pull down enabled

GpioOutEnB	5	1	0: Output enable 1: Output disable
GpioOut	6	0	Output state when GpioOutEnableB is enabled
GpioIn	7	0	Read only – current pin state

4.16.2.2 Address List

Default Configuration	GPIO#		Address
GPO3	GPIO224	0xFED80100 + GPIO224	0xFED801E0
GPO2	GPIO222	0xFED80100 + GPIO222	0xFED801DE
GPO1	GPIO220	0xFED80100 + GPIO220	0xFED801DC
GPO0	GPIO218	0xFED80100 + GPIO218	0xFED801DA
GPI3	GPIO215	0xFED80100 + GPIO215	0xFED801D7
GPI2	GPIO213	0xFED80100 + GPIO213	0xFED801D5
GPI1	GPIO211	0xFED80100 + GPIO211	0xFED801D3
GPI0	GPIO209	0xFED80100 + GPIO209	0xFED801D1

4.16.2.3 PSUEDO CODE

Example 1 *Change GPO2 from output to input*

```
Step1: ByteData = MemReadByte(0xFED801DE)   //Read current setting from configuration
                                            //Register
Step2: ByteData = ByteData | Bit 5          //Set Bit5 1. It means input
Step3: MemWriteByte(0xFED801DE, ByteData)   //Write back to configuration register
```

Example2 *Set GPO3 to output LOW*

```
Step1: ByteData = MemReadByte (0xFED801E0)   //Read current setting from Output Port
                                             //Register
Step2: ByteData =ByteData & 0x4F             //Set Bit6 0 It means output low
Step3: MemWriteByte (0xFED801E0, ByteData)   //Write back to Output Port Register
```

Example3 *Read GPI1*

```
Step1: ByteData = MemReadByte (0xFED801D3)   //Read current setting from GPI1
                                             //Register
Step2: ByteData = (ByteData & 0x80) >>7      //If ByteData = 1 It means input high
                                             //If ByteData = 0 It means input low
```

4.17 Power and System Management Signals

Signal	I/O	Description
SUS_S3#	O	Indicates system is suspended to RAM state. Active low output.
SUS_S4#	O	Indicates system is suspended to Disk state. Active low output.
SUS_S5#	O	Indicates system is in Soft Off state.
SUS_STAT#	O	Indicates imminent suspend operation.
PWRBTN#	I	Power button to bring system out of S5 (soft off), active on rising edge.
PWR_OK	I	Power OK from main power supply
BATLOW#	I	Indicates that external battery is low.
SYS_RESET#	I	Reset button input. Active low input.
CB_RESET#	O	Carrier Board Reset. Active low input.
WAKE0#	I	PCI Express wake up signal.
WAKE1#	I	General purpose wake up signal.
VCC_RTC	I	RTC External Battery
LID#	I	LID switch
SLEEP#	I	Sleep Button
FAN_PWMOUT	O	FAN PWM out
FAN_TACHIN	I	Fan Tacho in

4.18 Thermal Management Signals

Signal	I/O	Description
THRMTRIP#	O	Active low output indicating that the CPU has entered thermal shutdown.
THRM#	I	Input from off-module temp sensor indicating and over-temp situation.

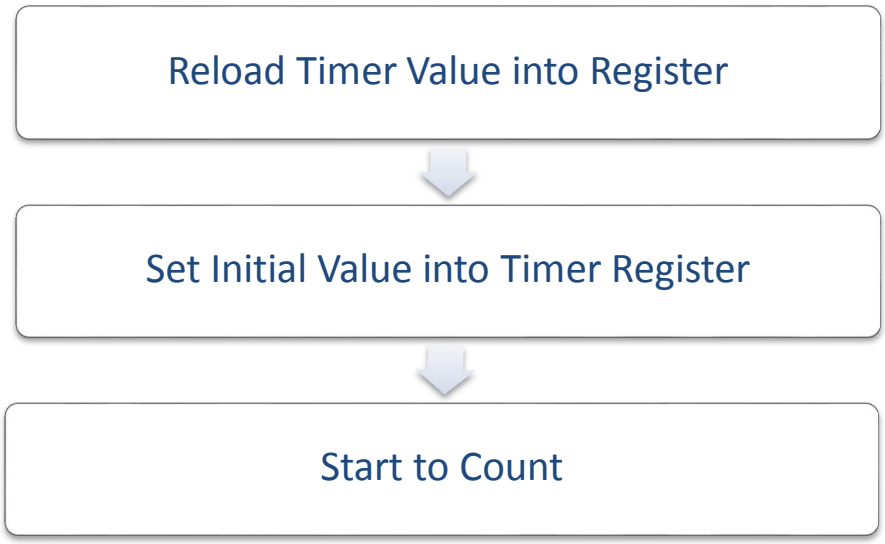
4.19 Miscellaneous Signals

Signal	I/O	Description
I2C_CK	O	General purpose I2C port clock output
I2C_DAT	I/O	General purpose I2C port data I/O lin
WDT	O	Indicator for Watchdog Timeout
SPKR	O	Output for audio enunciator-the “speaker” in PC-AT systems

Signal	I/O	Description
BIOS_DIS0# BIOS_DIS1#	I	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to the table below for strapping option of BIOS disable signals.

BIOS_DIS1#	BIOS_DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	BIOS Entry	Ref Line
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier FWH	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	0	Carrier	Module	SPI1	Module	SPI1/SPI1	3

4.20 Watchdog Timer



4.20.1 Board Design

The WDT (Watchdog Timer) is implemented by using Fintek Super I/O(F81801).

Register	Address
I/O Base (BaseAddress)	0x500

4.20.2 Watchdog Timer Configuration

BaseAddress + 5

Bit	Name	Default	Description
7	Reserved	0	Reserved
6	WDTMOUT_STS	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	0	Select output mode (0: level, 1: pulse)
3	WD_UNIT	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	0	Select output polarity (1: high active, 0: low active)
1:0	WD_PSWIDTH	0	Select output pulse width 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

BaseAddress + 6

Bit	Name	Default	Description
7:0	WD_TIME	0	Time of watchdog timer

4.20.3 PSUEDO CODE

Example 1 WDT set to 7 sec

Step1: WriteIOByte(0x506, 0x07) //Set timer to 7
Step2: WriteIOByte(0x505, 0x31) //Select output mode is pulse bit4 to 1
//Select timer unit is sec bit3 to 0
//Select pulse width bit1:0 to 1
//Enable WDT bit5 to 1

Note:
Suggest pulse width is more than 25ms, because not all of chipset can accept 1ms pulse.

Example 2 WDT set to 1 min

Step1: WriteIOByte(0x506, 0x01) //Set timer
Step2: WriteIOByte(0x505, 0x39) //Select output mode is pulse bit4 to 1
//Select timer unit is sec bit3 to 1
//Select pulse width bit1:0 to 1

//Enable WDT bit5 to 1

Note:

Suggest pulse width is more than 25ms, because not all of chipset can accept 1ms pulse.

V. SYSTEM BIOS

The system BIOS software is stored on EEPROM. The BIOS provides an interface to modify the configuration. When the battery is removed, all the parameters will be reset.

Turn on the computer and press <DEL> or <F2> to enter the setup screens.

5.1 Main

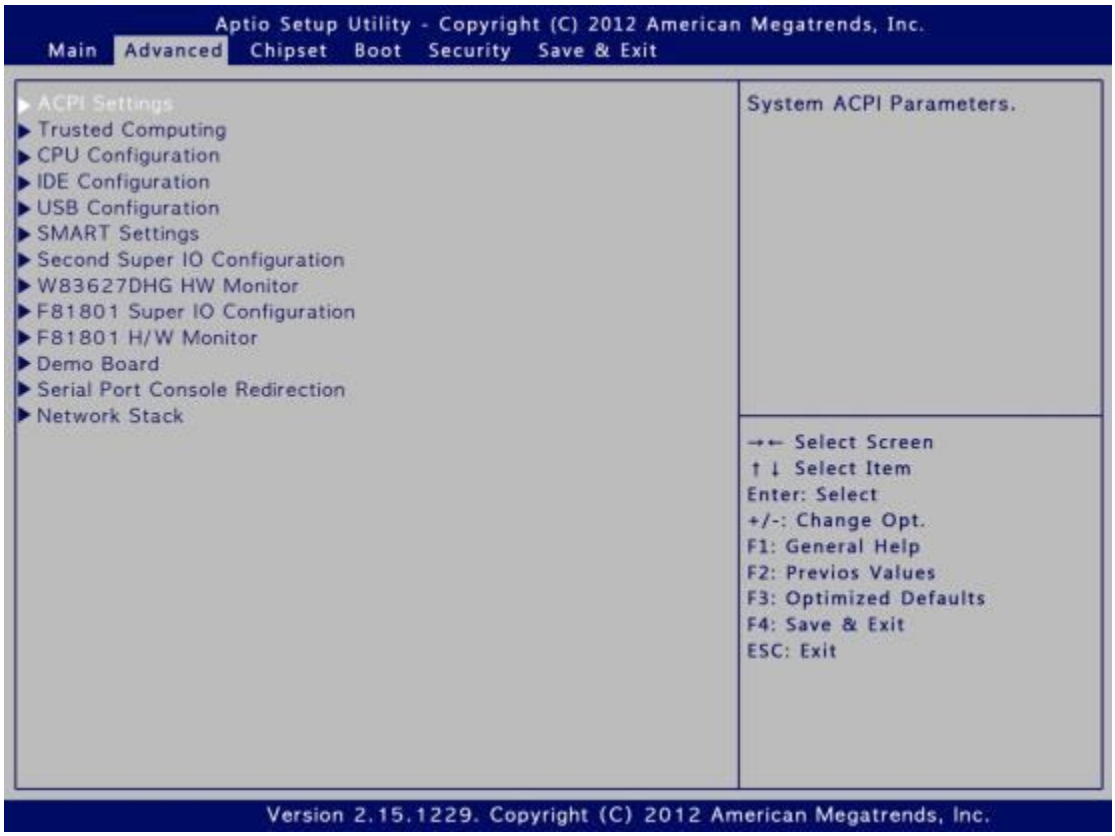
The Main setup screen is showed as following when the setup utility is entered. System Date/Time is set up in the Main Menu.

System Language: Choose the system default language

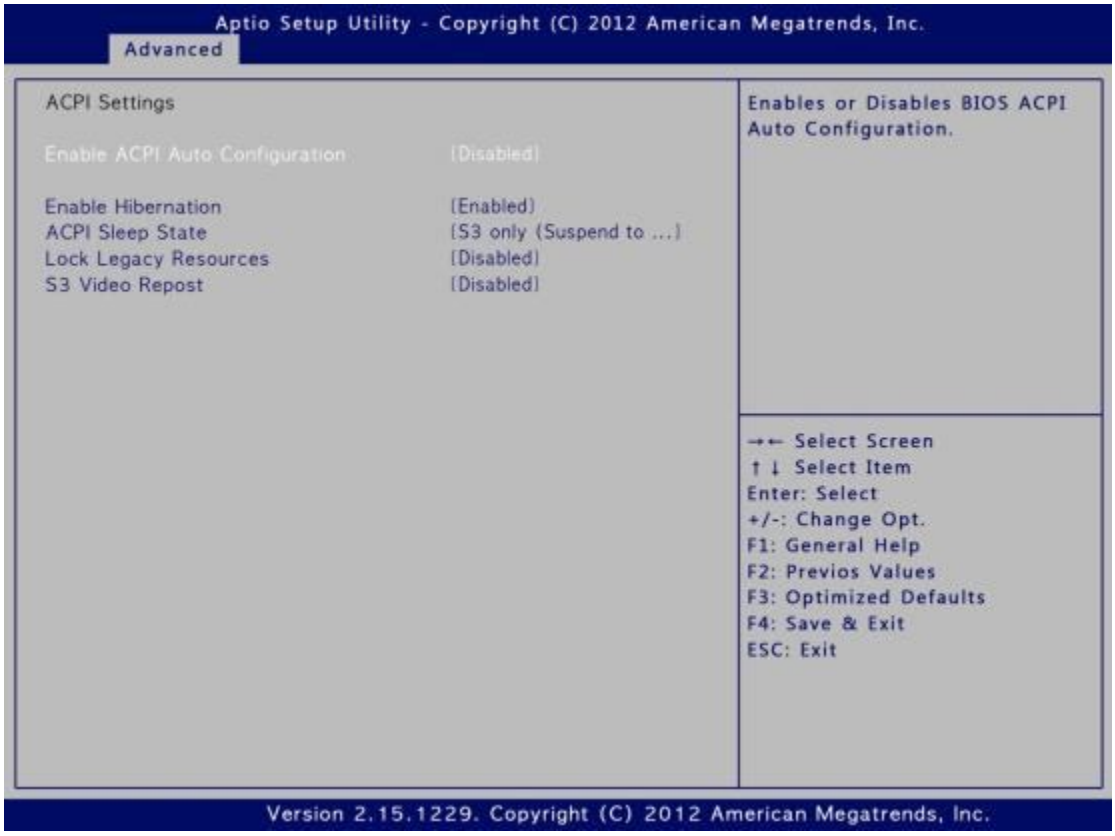
System Date: MM/DD/YYYY. Set the Date. Use Tab to switch between Date elements.

System Time: HH:MM:SS. Set the Time. Use Tab to switch between Time elements.

5.2 Advanced


Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc.
Main
Advanced
Chipset
Boot
Security
Save & Exit
ACPI Settings
Trusted Computing
CPU Configuration
IDE Configuration
USB Configuration
SMART Settings
Second Super IO Configuration
W83627DHG HW Monitor
F81801 Super IO Configuration
F81801 H/W Monitor
Demo Board
Serial Port Console Redirection
Network Stack
System ACPI Parameters.
→← Select Screen
↑↓ Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previos Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.

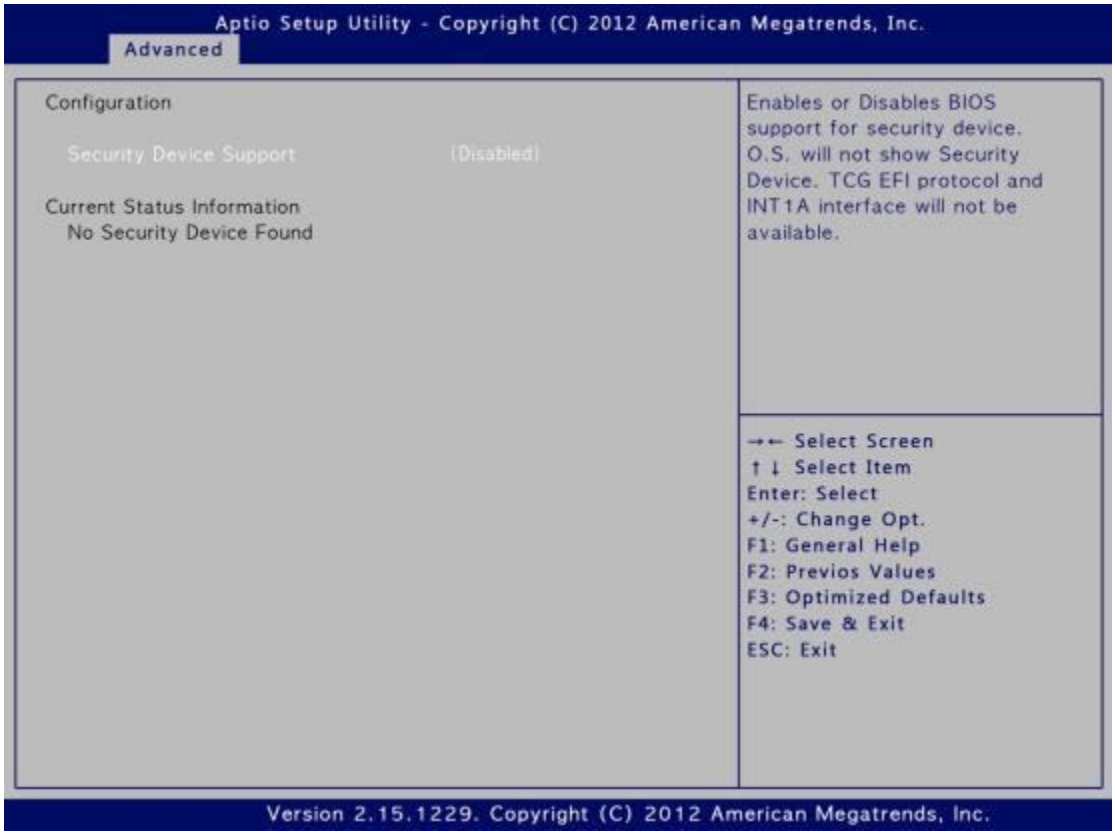
5.2.1 ACPI Settings



Enable ACPI Auto Configuration: Enable or Disable BIOS ACPI Auto Configuration.

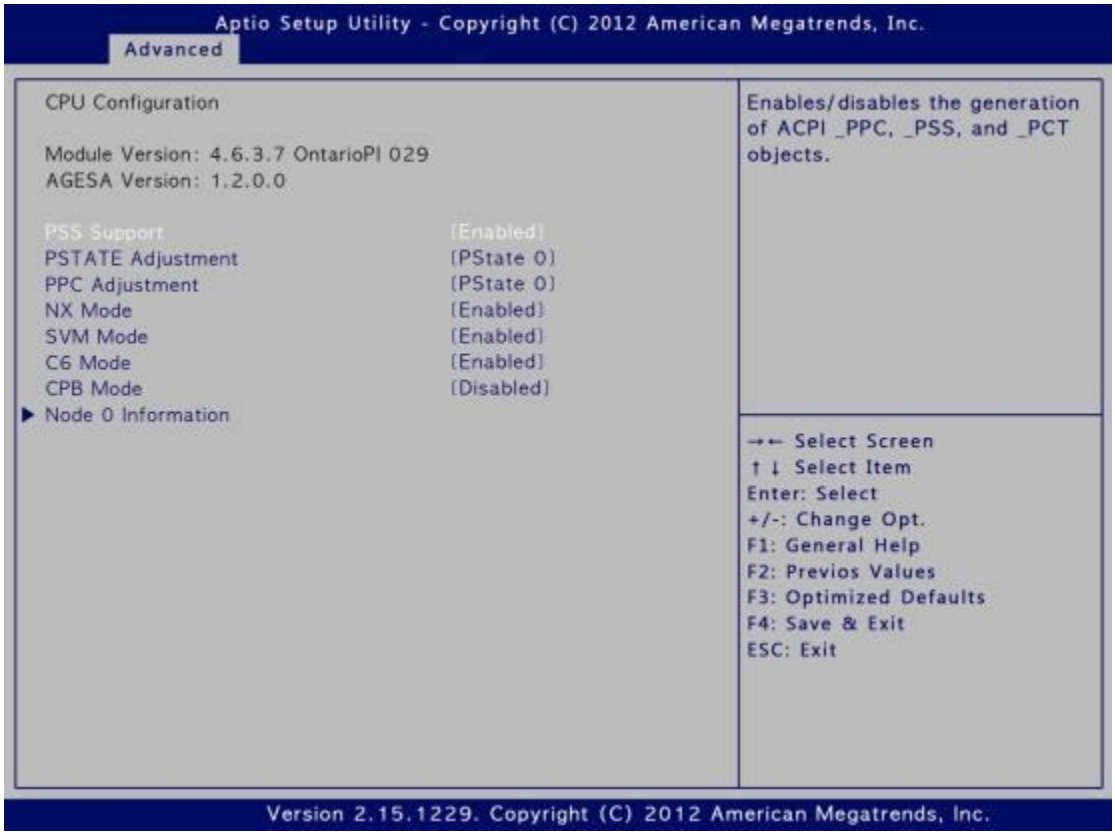
ACPI Sleep State: Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Select between [Suspend Disabled], [S1 (CPU Stop Clock)] and [S3 (Suspend to RAM)].

5.2.2 Trusted Computing



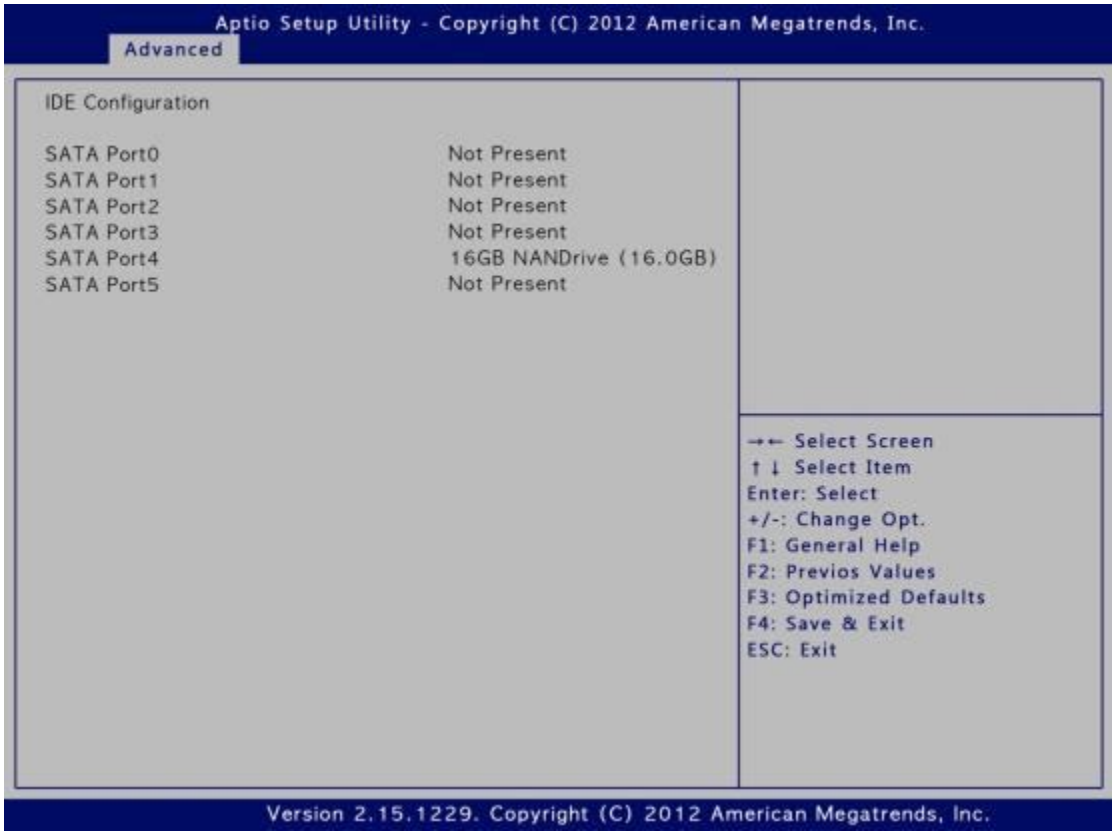
Security Device Support enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

5.2.3 CPU Configuration

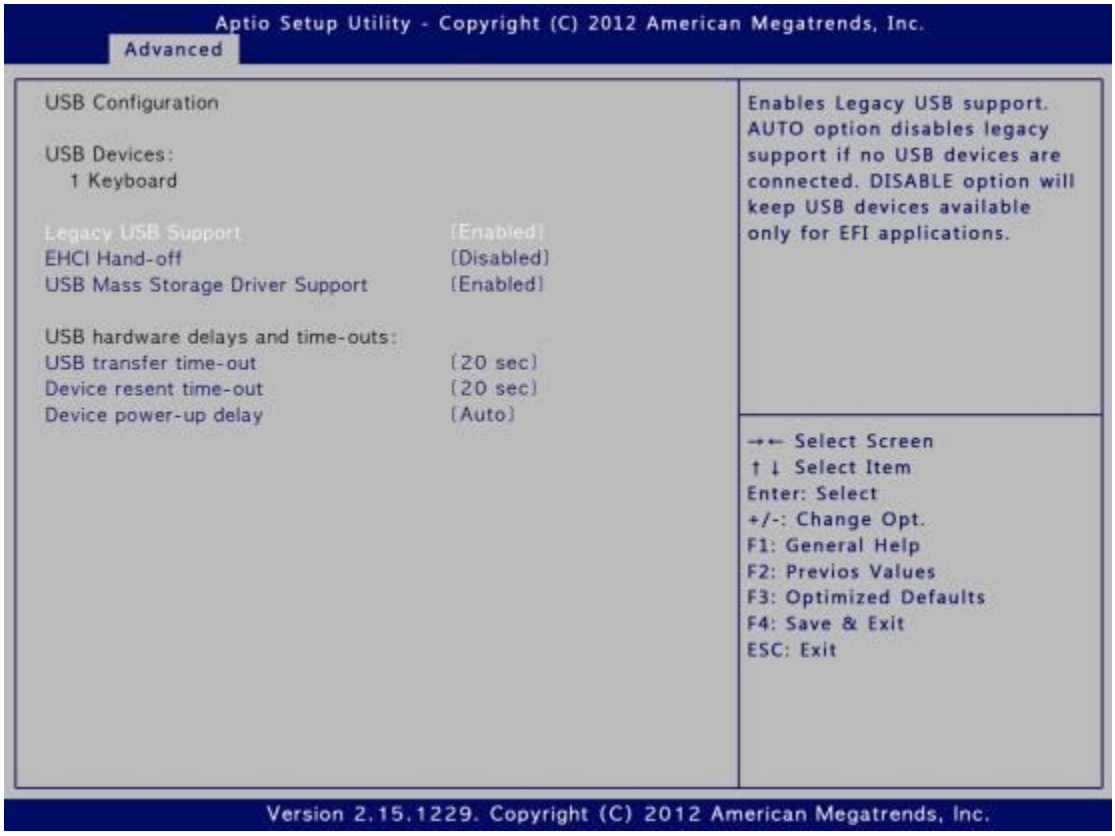


5.2.4 IDE Configuration

The BIOS automatically detects the presence of SATA device and the hardware installed in the SATA ports will be showed in the configuration.



5.2.5 USB Configuration

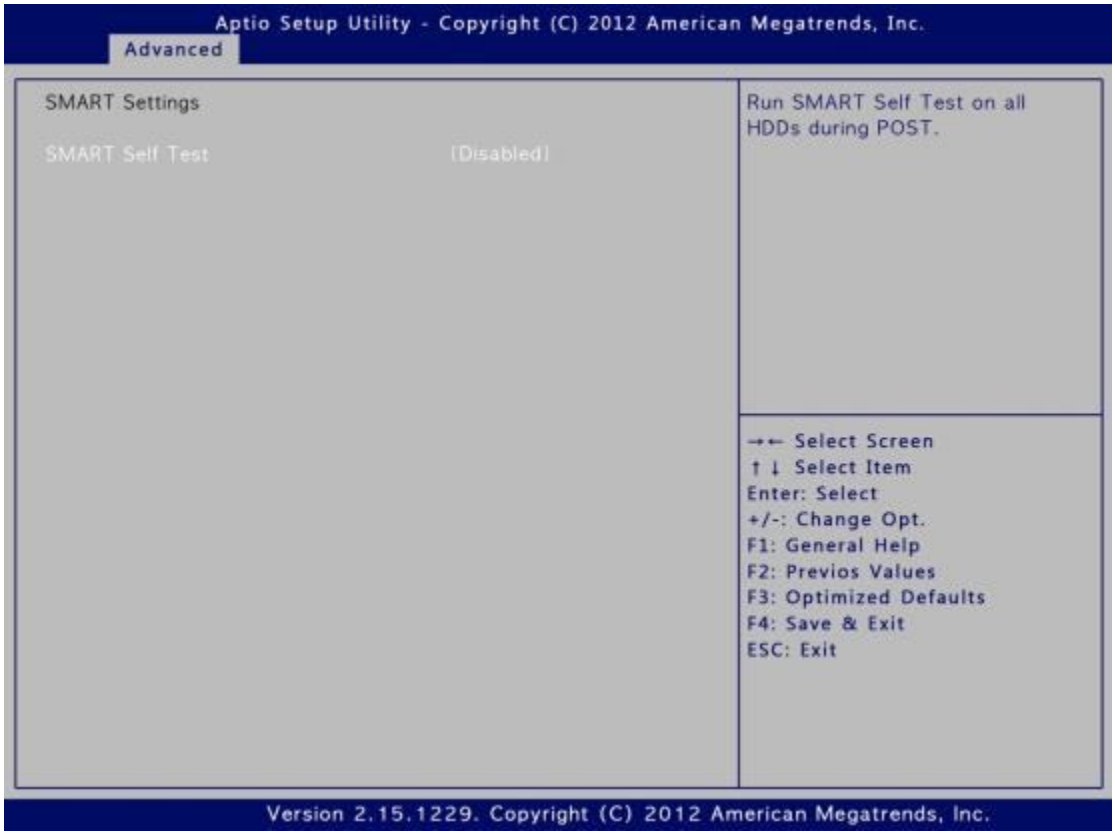


Legacy USB Support: AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

EHCI Hand-off: This is a workaround for OS without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB transfer time-out: Select between [1 sec], [5 sec], [10 sec] or [20 sec].

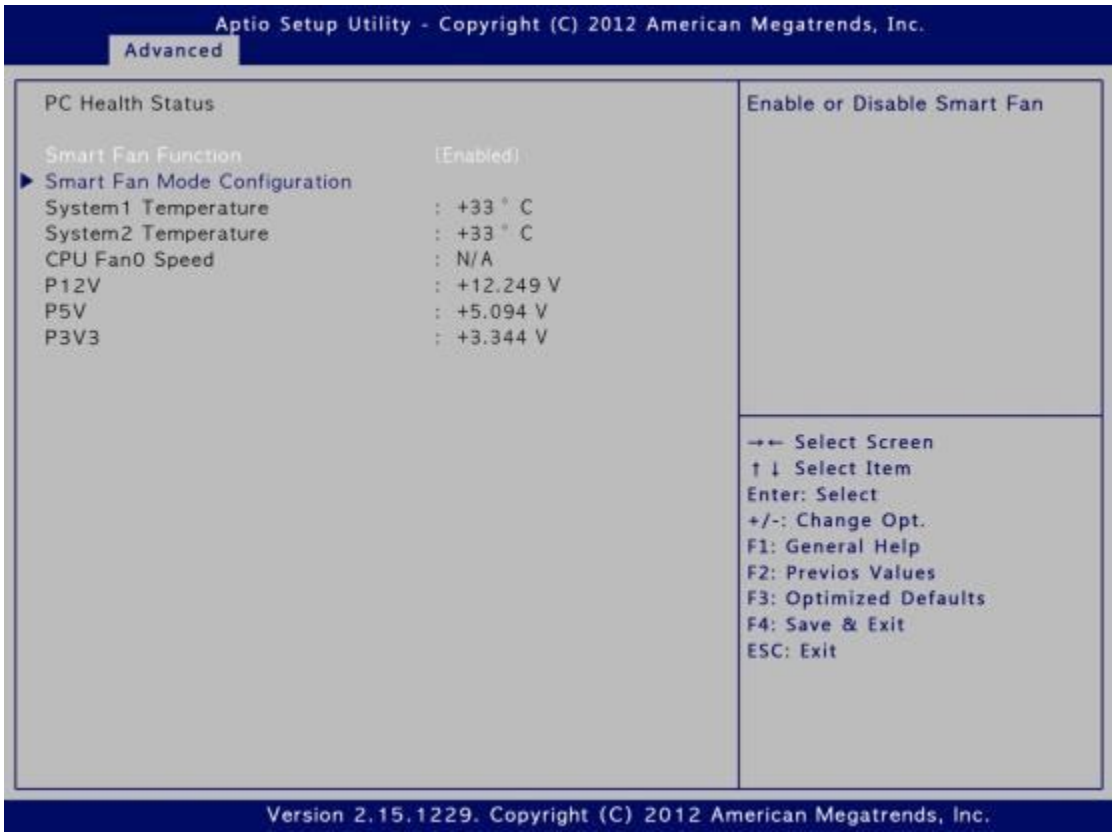
5.2.6 SMART Settings



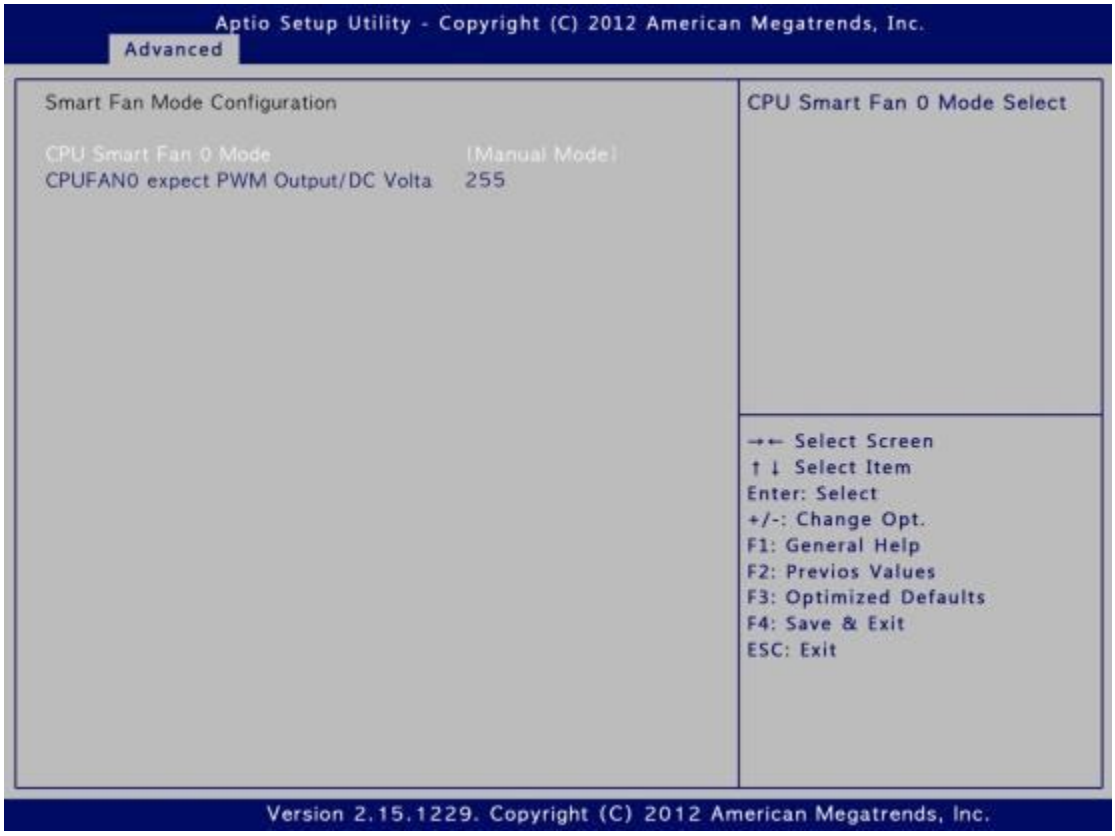
5.2.7 Second Super IO Configuration

Two serial ports could be configured.

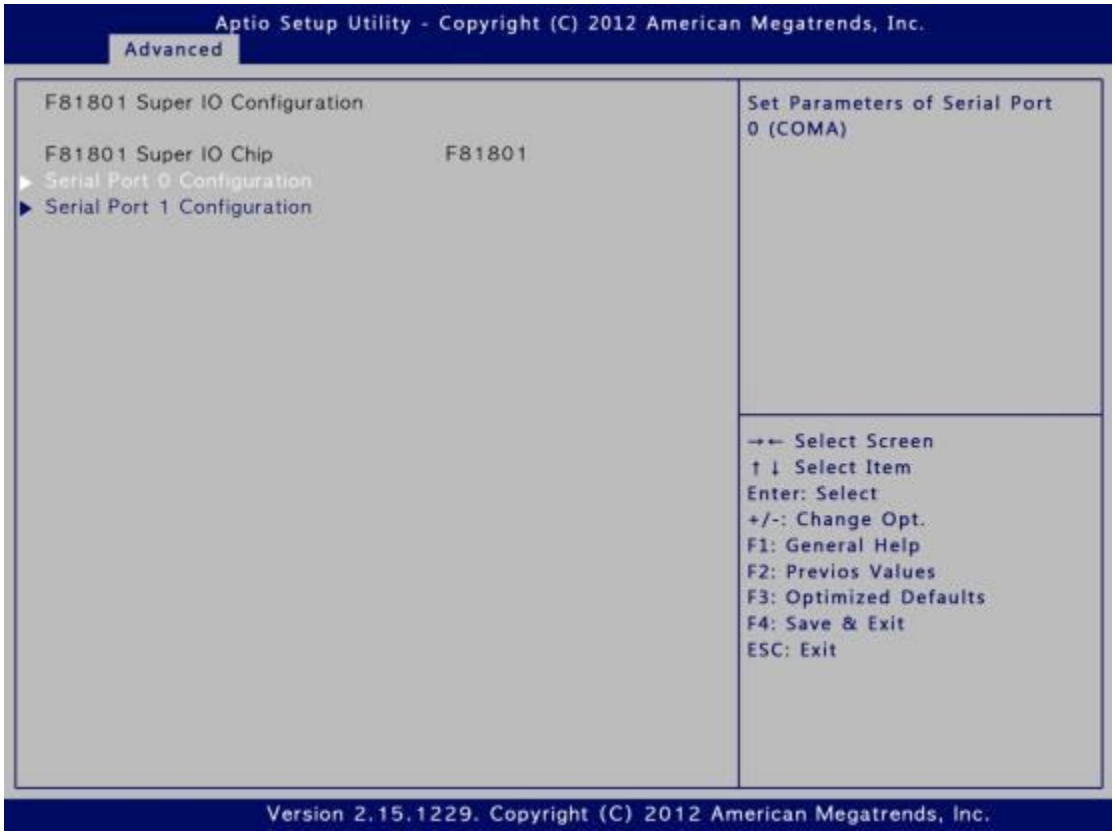
5.2.8 W83627DHG Hardware Monitor



5.2.8.1 Smart Fan Mode Configuration

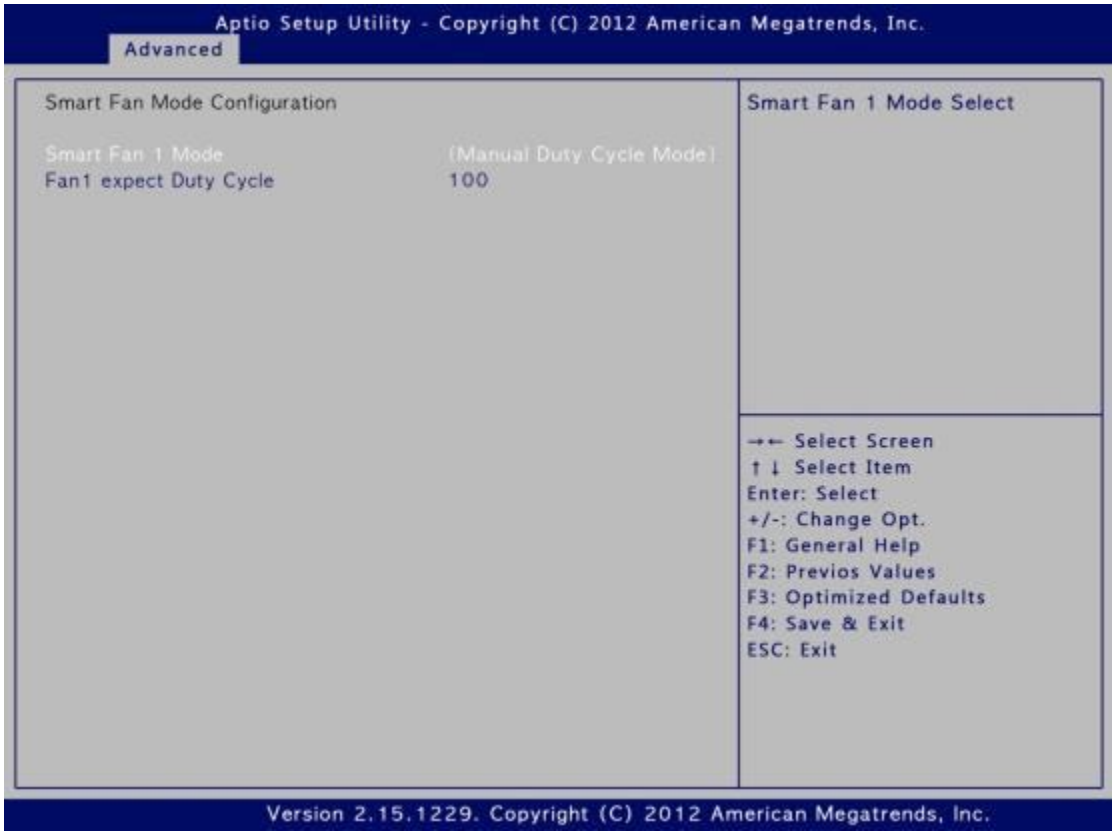


5.2.9 F81801 Super IO Configuration



5.2.10 F81801 H/W Monitor

5.2.10.1 Smart Fan Mode Configuration

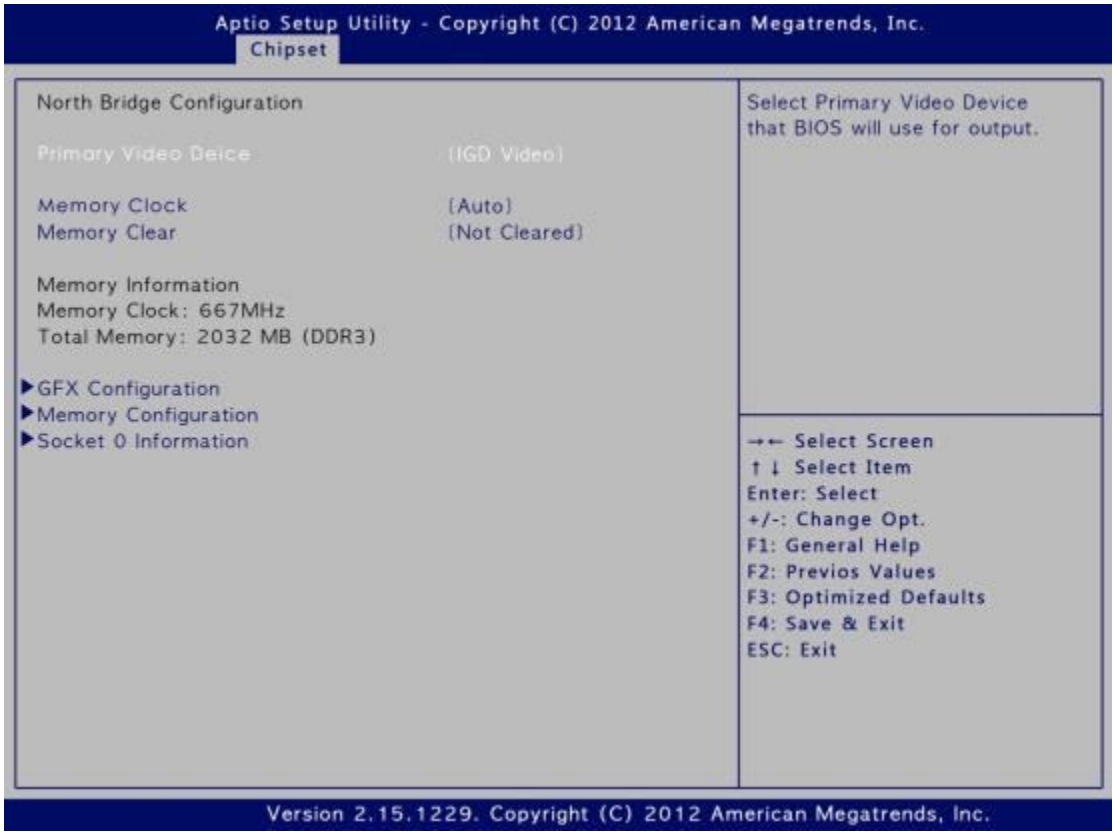


5.2.11 Serial Port Console Redirection

5.3 Chipset


Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
North Bridge
North Bridge Display Config Select
South Bridge
North Bridge Parameters
→← Select Screen
↑↓ Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previos Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.

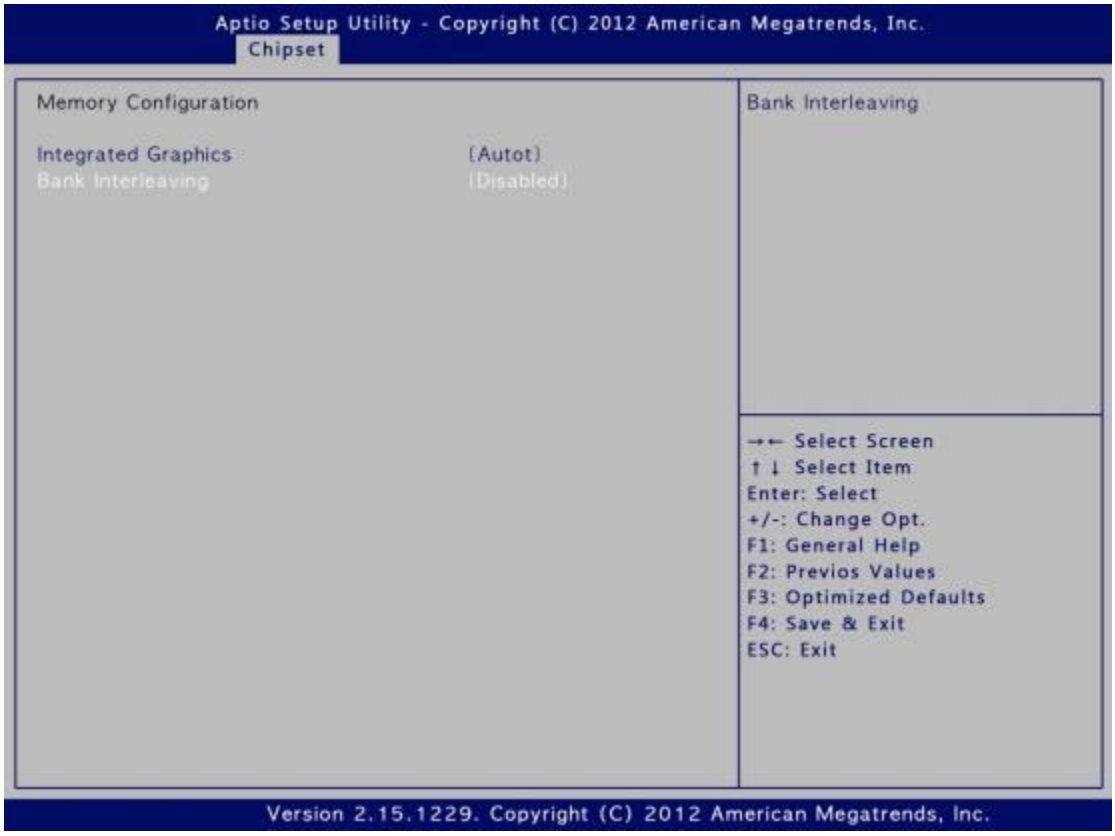
5.3.1 North Bridge



5.3.1.1 GFX Configuration

NB GPP Core Config: Select between [Disabled], [GPP_CORE_x4x4], [GPP_CORE_x4x2x2], [GPP_CORE_x4x2x1x1] and [GPP_CORE_x4x1x1x1x1].

5.3.1.2 Memory Configuration

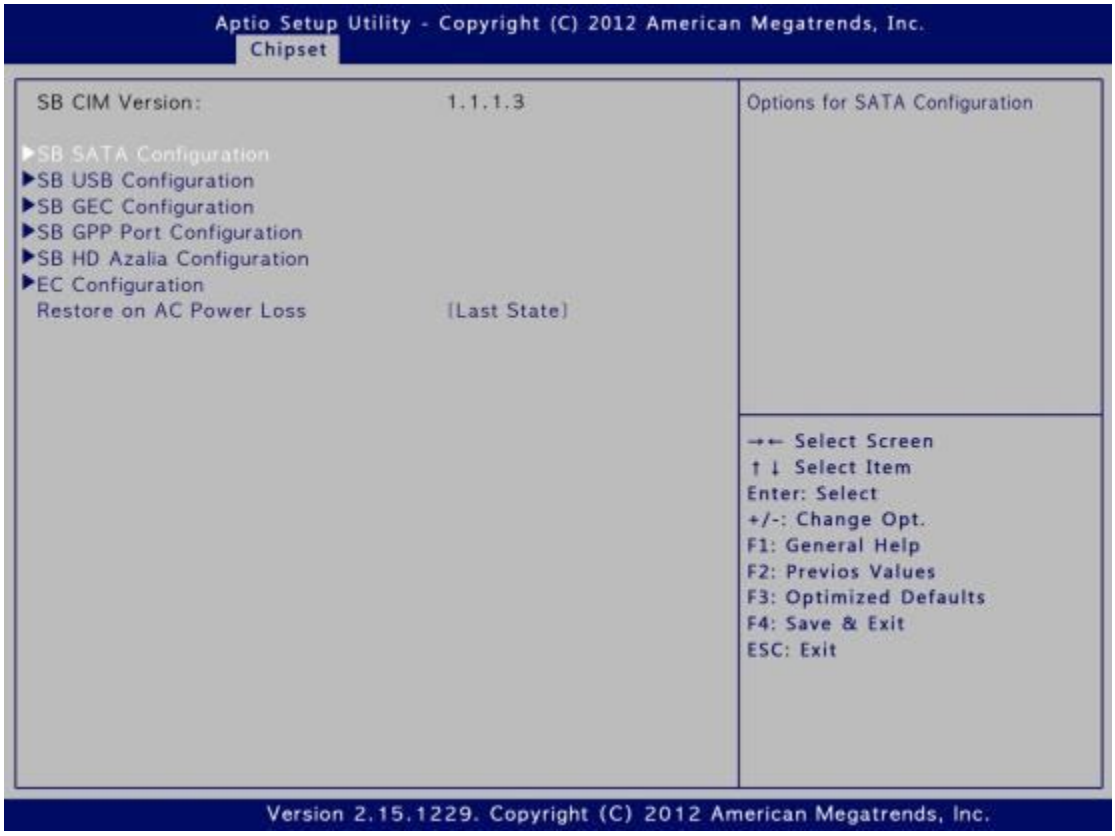


5.3.2 North Bridge Display Config Select

DP0 Output Mode: The type of display device that NB PCIe connects to. If LVDS Panel is used, there will be a LVDS Panel Configuration selection:

1-ch, 18bit 640x480
1-ch, 18bit 800x600
1-ch, 18bit 1024x600
1-ch, 18bit 1024x768
1-ch, 18bit 1280x800
1-ch, 18bit 1366x768
1-ch, 24bit 1024x768
1-ch, 24bit 1366x768
2-ch, 24bit 1280x1024
2-ch, 24bit 1440x900
2-ch, 24bit 1440x1050
2-ch, 24bit 1600x900
2-ch, 24bit 1600x1200
2-ch, 24bit 1680x1050
2-ch, 24bit 1920x1080
2-ch, 24bit 1920x1200

5.3.3 South Bridge



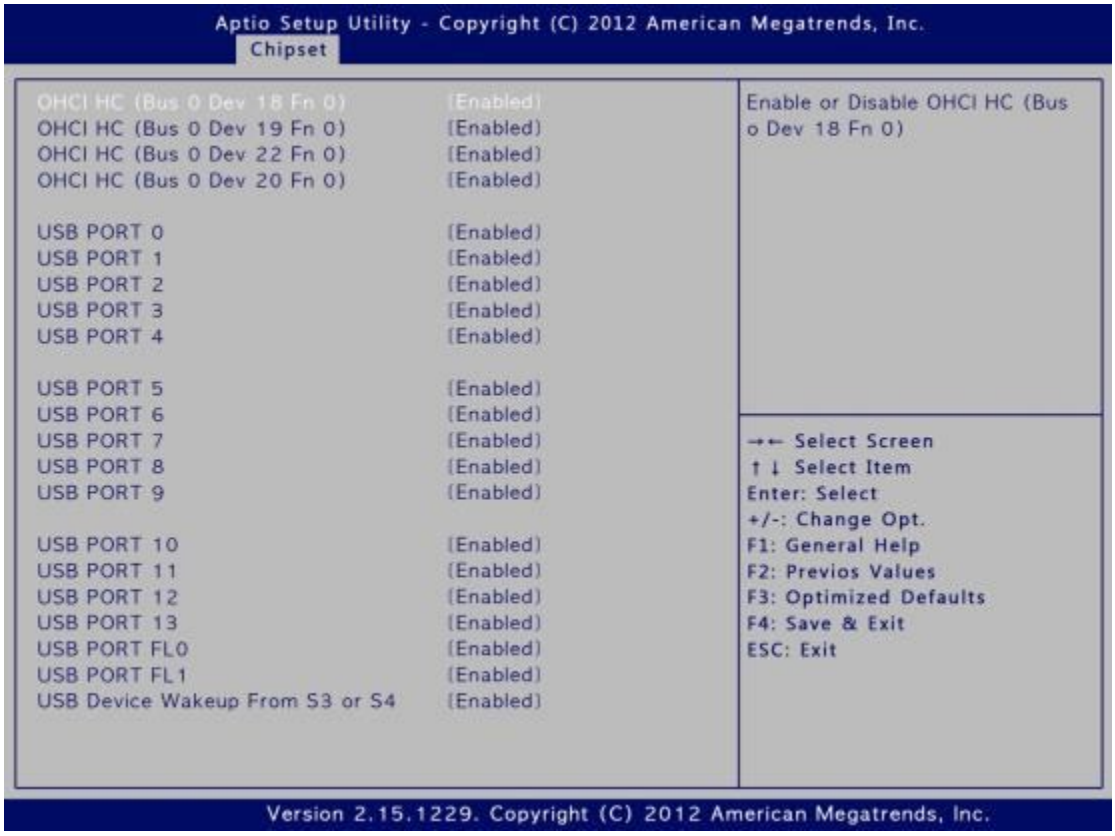
5.3.3.1 SB SATA Configuration

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc.
Chipset

OnChip SATA Channel	[Enabled]	Enable or Disable Serial ATA
OnChip SATA Type	[AHCI]	
OnChip IDE mode	[Legacy mode]	
SATA IDE Combined Mode	[Disabled]	
SATA ESP on PORT0	[Disabled]	
SATA ESP on PORT1	[Disabled]	
SATA ESP on PORT2	[Disabled]	
SATA ESP on PORT3	[Disabled]	
SATA ESP on PORT4	[Disabled]	
SATA ESP on PORT5	[Disabled]	
SATA Power on PORT0	[Enabled]	
SATA Power on PORT1	[Enabled]	
SATA Power on PORT2	[Enabled]	→← Select Screen
SATA Power on PORT3	[Enabled]	↑↓ Select Item
SATA Power on PORT4	[Enabled]	Enter: Select
SATA Power on PORT5	[Enabled]	+/-: Change Opt.
		F1: General Help
		F2: Previos Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit

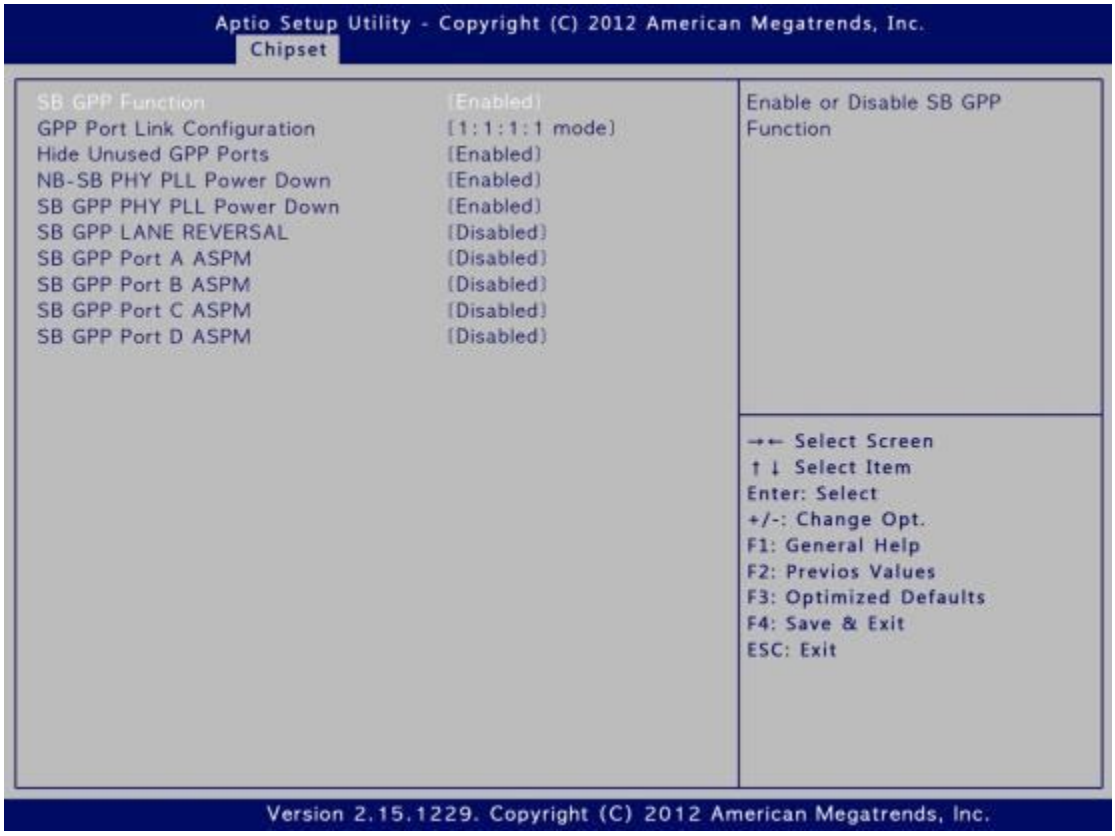
Version 2.15.1229. Copyright (C) 2012 American Megatrends, Inc.

5.3.3.2 SB USB Configuration



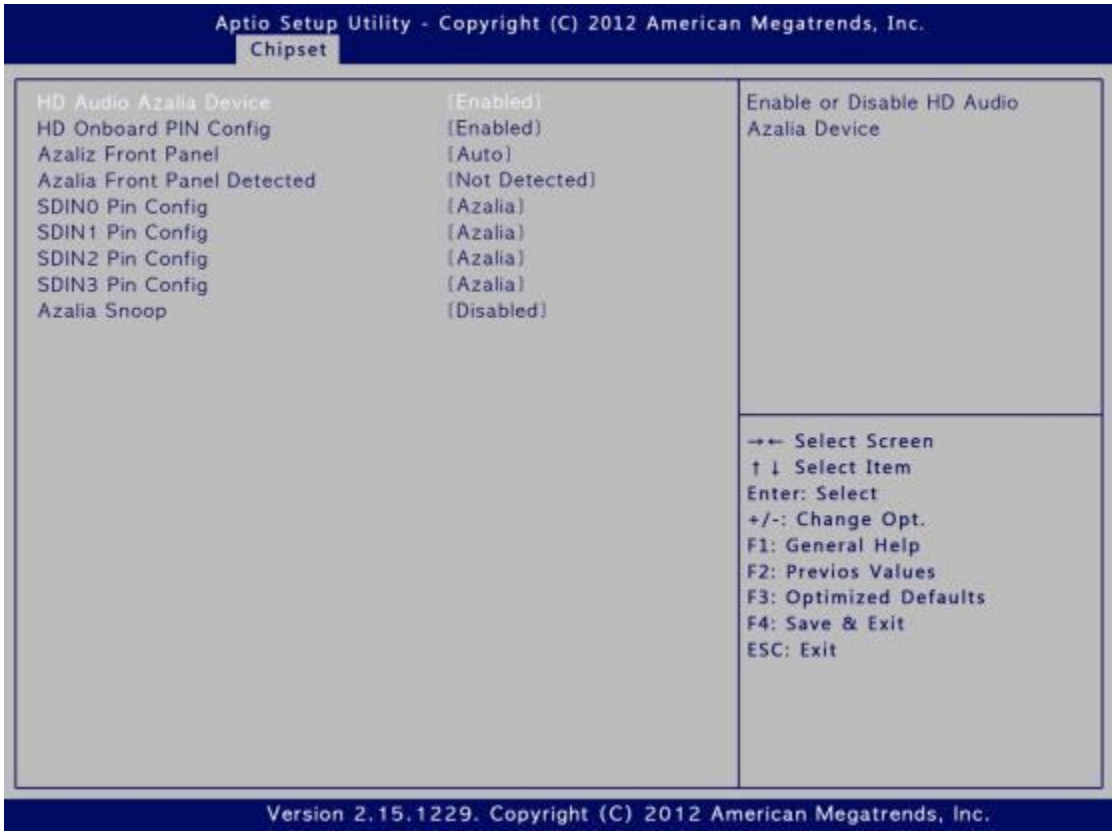
5.3.3.3 SB GEC Configuration

5.3.3.4 SB GPP Port Configuration

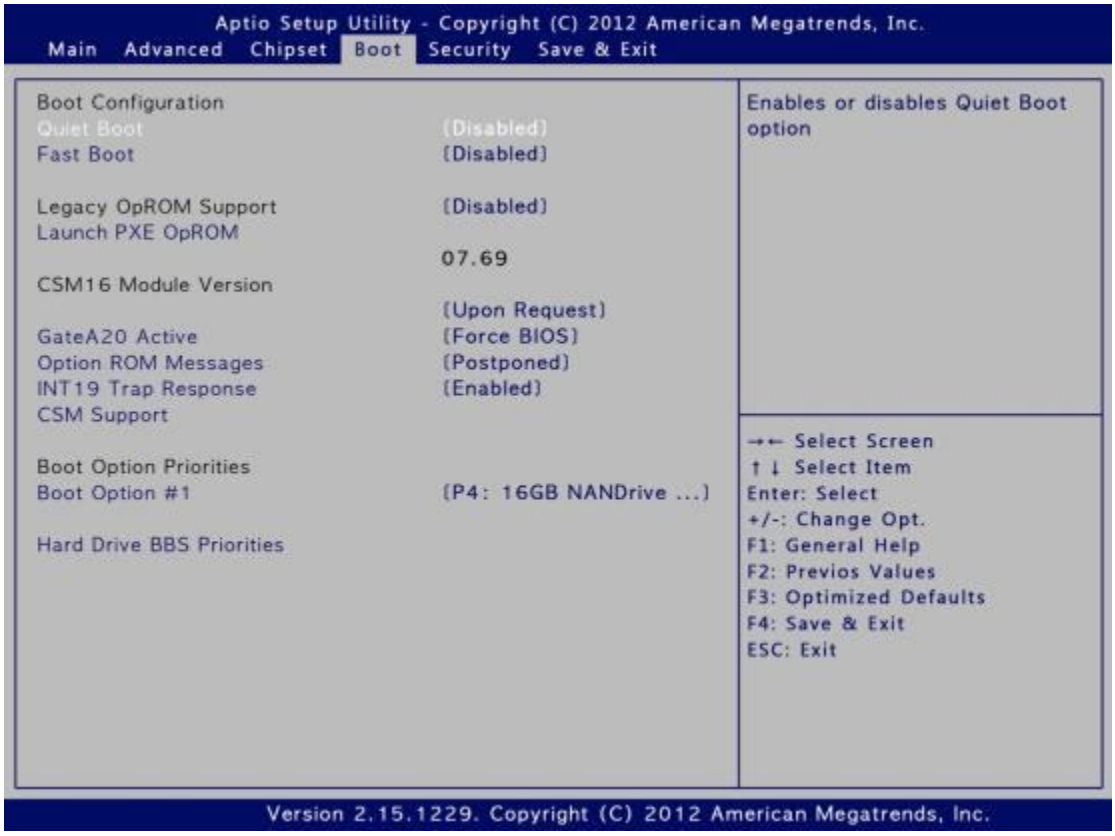


GPP Port Link Configuration: It can be select between [x4 mode], [2:2 mode], [2:1:1 mode] and [1:1:1:1 mode].

5.3.3.5 SB HD Azalia Configuration



5.4 Boot



Quiet Boot: Enables or disables Quiet Boot option.

GateA20 Active:

[Upon Request] – GA20 can be disabled using BIOS services.

[Always] – do not allow disabling GA20; this option is useful wen any RT code is executed above 1MB.

Option ROM Message: Set display mode [Force BIOS] or [Keep Current] for Option ROM.

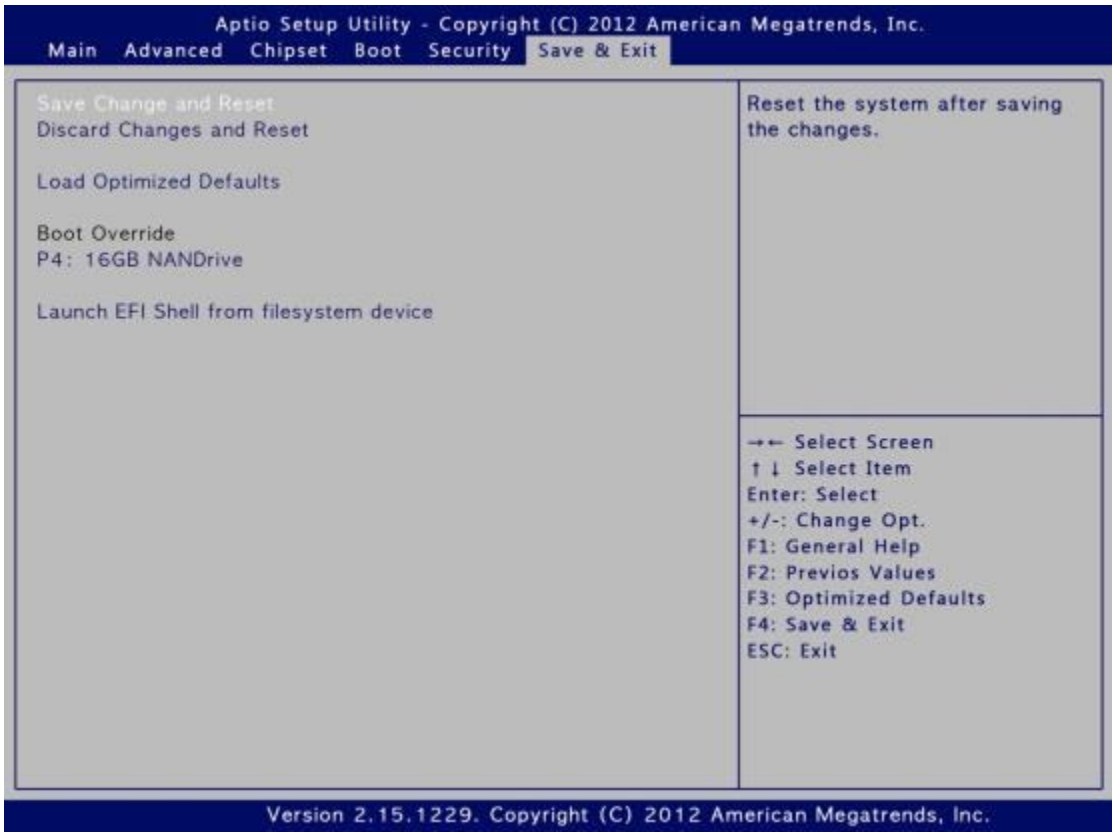
Boot Option #1: Set the system boot order.

Hard Drive BBS Priorities: Set the order of the legacy devices in this group.

5.5 Security

Administrator's and User's passwords could be set.
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup, the user will have administrator rights. The minimum length of the password is 3 and the maximum length is 20.

5.6 Save and Exit



Save Changes and Exit: Exit system setup after saving the changes.
Discard Changes and Exit: Exit system setup without saving any changes.
Save Changes and Reset: Reset the system after saving the changes.
Discard Changes and Reset: Reset system setup without saving any changes.
Save Changes: Save Changes done so far to any of the setup options.
Discard Changes: Discard Changes done so far to any of the setup options.
Restore Defaults: Restore/Load Default values for all the setup options.
Save as User Defaults: Save the changes done so far as user Defaults.
Restore user Defaults: Restore the User Defaults to all the setup options.
Launch EFI Shell from filesystem device: Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available filesystem devices.

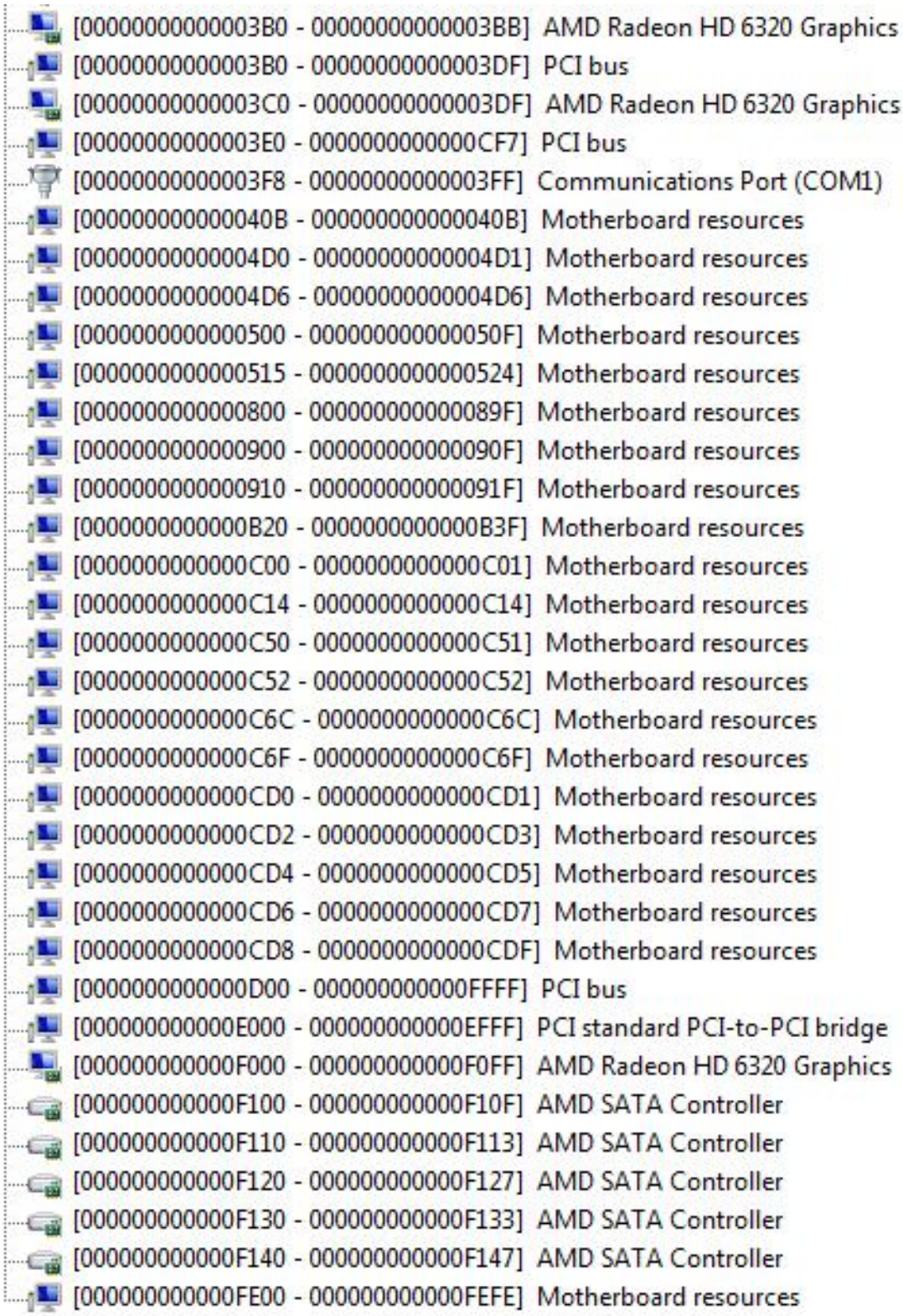
VI. Address Map

6.1 I/O Port Address Map

The assignment of the I/O port addresses for the CT-CA56X with CT-BT601 carrier board under Windows® 7 Ultimate/64bit are shown below.

Input/output (IO)

- [0000000000000000 - 000000000000000F] Direct memory access controller
- [0000000000000000 - 000000000000000F] Motherboard resources
- [0000000000000000 - 00000000000003AF] PCI bus
- [0000000000000010 - 000000000000001F] Motherboard resources
- [0000000000000020 - 000000000000021] Programmable interrupt controller
- [0000000000000022 - 000000000000003F] Motherboard resources
- [0000000000000040 - 000000000000043] System timer
- [0000000000000044 - 000000000000005F] Motherboard resources
- [0000000000000060 - 000000000000060] Microsoft PS/2 Mouse
- [0000000000000061 - 000000000000061] System speaker
- [0000000000000062 - 000000000000063] Motherboard resources
- [0000000000000064 - 000000000000064] Microsoft PS/2 Mouse
- [0000000000000065 - 000000000000006F] Motherboard resources
- [0000000000000070 - 000000000000071] System CMOS/real time clock
- [0000000000000072 - 000000000000007F] Motherboard resources
- [0000000000000080 - 000000000000080] Motherboard resources
- [0000000000000081 - 000000000000083] Direct memory access controller
- [0000000000000084 - 000000000000086] Motherboard resources
- [0000000000000087 - 000000000000087] Direct memory access controller
- [0000000000000088 - 000000000000088] Motherboard resources
- [0000000000000089 - 00000000000008B] Direct memory access controller
- [000000000000008C - 000000000000008E] Motherboard resources
- [000000000000008F - 000000000000008F] Direct memory access controller
- [0000000000000090 - 000000000000009F] Motherboard resources
- [00000000000000A0 - 00000000000000A1] Programmable interrupt controller
- [00000000000000A2 - 00000000000000BF] Motherboard resources
- [00000000000000C0 - 00000000000000DF] Direct memory access controller
- [00000000000000E0 - 00000000000000EF] Motherboard resources
- [00000000000000F0 - 00000000000000FF] Numeric data processor
- [0000000000000228 - 000000000000022F] Communications Port (COM4)
- [0000000000000238 - 000000000000023F] Communications Port (COM3)
- [00000000000002F8 - 00000000000002FF] Communications Port (COM2)


[00000000000003B0 - 00000000000003BB] AMD Radeon HD 6320 Graphics
[00000000000003B0 - 00000000000003DF] PCI bus
[00000000000003C0 - 00000000000003DF] AMD Radeon HD 6320 Graphics
[00000000000003E0 - 0000000000000CF7] PCI bus
[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
[000000000000040B - 000000000000040B] Motherboard resources
[00000000000004D0 - 00000000000004D1] Motherboard resources
[00000000000004D6 - 00000000000004D6] Motherboard resources
[0000000000000500 - 000000000000050F] Motherboard resources
[0000000000000515 - 0000000000000524] Motherboard resources
[0000000000000800 - 000000000000089F] Motherboard resources
[0000000000000900 - 000000000000090F] Motherboard resources
[0000000000000910 - 000000000000091F] Motherboard resources
[0000000000000B20 - 0000000000000B3F] Motherboard resources
[0000000000000C00 - 0000000000000C01] Motherboard resources
[0000000000000C14 - 0000000000000C14] Motherboard resources
[0000000000000C50 - 0000000000000C51] Motherboard resources
[0000000000000C52 - 0000000000000C52] Motherboard resources
[0000000000000C6C - 0000000000000C6C] Motherboard resources
[0000000000000C6F - 0000000000000C6F] Motherboard resources
[0000000000000CD0 - 0000000000000CD1] Motherboard resources
[0000000000000CD2 - 0000000000000CD3] Motherboard resources
[0000000000000CD4 - 0000000000000CD5] Motherboard resources
[0000000000000CD6 - 0000000000000CD7] Motherboard resources
[0000000000000CD8 - 0000000000000CDF] Motherboard resources
[0000000000000D00 - 000000000000FFFF] PCI bus
[000000000000E000 - 000000000000EFFF] PCI standard PCI-to-PCI bridge
[000000000000F000 - 000000000000F0FF] AMD Radeon HD 6320 Graphics
[000000000000F100 - 000000000000F10F] AMD SATA Controller
[000000000000F110 - 000000000000F113] AMD SATA Controller
[000000000000F120 - 000000000000F127] AMD SATA Controller
[000000000000F130 - 000000000000F133] AMD SATA Controller
[000000000000F140 - 000000000000F147] AMD SATA Controller
[000000000000FE00 - 000000000000FEFE] Motherboard resources

6.2 Interrupt Controller (IRQ) Map

The interrupt controller map for the CT-CA56X with the CT-BT601 carrier board under Windows® 7 Ultimate/64bit are as shown below.

Interrupt request (IRQ)

(ISA) 0x00000000 (00)	System timer
(ISA) 0x00000003 (03)	Communications Port (COM2)
(ISA) 0x00000004 (04)	Communications Port (COM1)
(ISA) 0x00000008 (08)	System CMOS/real time clock
(ISA) 0x0000000A (10)	Communications Port (COM4)
(ISA) 0x0000000B (11)	Communications Port (COM3)
(ISA) 0x0000000C (12)	Microsoft PS/2 Mouse
(ISA) 0x0000000D (13)	Numeric data processor
(ISA) 0x00000051 (81)	Microsoft ACPI-Compliant System
(ISA) 0x00000052 (82)	Microsoft ACPI-Compliant System
(ISA) 0x00000053 (83)	Microsoft ACPI-Compliant System
(ISA) 0x00000054 (84)	Microsoft ACPI-Compliant System
(ISA) 0x00000055 (85)	Microsoft ACPI-Compliant System
(ISA) 0x00000056 (86)	Microsoft ACPI-Compliant System
(ISA) 0x00000057 (87)	Microsoft ACPI-Compliant System
(ISA) 0x00000058 (88)	Microsoft ACPI-Compliant System
(ISA) 0x00000059 (89)	Microsoft ACPI-Compliant System
(ISA) 0x0000005A (90)	Microsoft ACPI-Compliant System
(ISA) 0x0000005B (91)	Microsoft ACPI-Compliant System
(ISA) 0x0000005C (92)	Microsoft ACPI-Compliant System
(ISA) 0x0000005D (93)	Microsoft ACPI-Compliant System
(ISA) 0x0000005E (94)	Microsoft ACPI-Compliant System
(ISA) 0x0000005F (95)	Microsoft ACPI-Compliant System
(ISA) 0x00000060 (96)	Microsoft ACPI-Compliant System
(ISA) 0x00000061 (97)	Microsoft ACPI-Compliant System
(ISA) 0x00000062 (98)	Microsoft ACPI-Compliant System
(ISA) 0x00000063 (99)	Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100)	Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101)	Microsoft ACPI-Compliant System
(ISA) 0x00000066 (102)	Microsoft ACPI-Compliant System
(ISA) 0x00000067 (103)	Microsoft ACPI-Compliant System
(ISA) 0x00000068 (104)	Microsoft ACPI-Compliant System
(ISA) 0x00000069 (105)	Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106)	Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107)	Microsoft ACPI-Compliant System
(ISA) 0x0000006C (108)	Microsoft ACPI-Compliant System
(ISA) 0x0000006D (109)	Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110)	Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111)	Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112)	Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113)	Microsoft ACPI-Compliant System

(ISA) 0x00000072 (114)	Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115)	Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116)	Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117)	Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118)	Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119)	Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120)	Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121)	Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122)	Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123)	Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124)	Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125)	Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126)	Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127)	Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128)	Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129)	Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130)	Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131)	Microsoft ACPI-Compliant System
(ISA) 0x00000084 (132)	Microsoft ACPI-Compliant System
(ISA) 0x00000085 (133)	Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134)	Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135)	Microsoft ACPI-Compliant System
(ISA) 0x00000088 (136)	Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137)	Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138)	Microsoft ACPI-Compliant System
(ISA) 0x0000008B (139)	Microsoft ACPI-Compliant System
(ISA) 0x0000008C (140)	Microsoft ACPI-Compliant System
(ISA) 0x0000008D (141)	Microsoft ACPI-Compliant System
(ISA) 0x0000008E (142)	Microsoft ACPI-Compliant System
(ISA) 0x0000008F (143)	Microsoft ACPI-Compliant System
(ISA) 0x00000090 (144)	Microsoft ACPI-Compliant System
(ISA) 0x00000091 (145)	Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146)	Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147)	Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148)	Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149)	Microsoft ACPI-Compliant System
(ISA) 0x00000096 (150)	Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151)	Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152)	Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153)	Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154)	Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155)	Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156)	Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157)	Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158)	Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159)	Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160)	Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161)	Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162)	Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163)	Microsoft ACPI-Compliant System

(ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
(ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
(ISA) 0x000000A8 (168) Microsoft ACPI-Compliant System
(ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
(ISA) 0x000000AA (170) Microsoft ACPI-Compliant System
(ISA) 0x000000AB (171) Microsoft ACPI-Compliant System
(ISA) 0x000000AC (172) Microsoft ACPI-Compliant System
(ISA) 0x000000AD (173) Microsoft ACPI-Compliant System
(ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
(ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
(ISA) 0x000000B0 (176) Microsoft ACPI-Compliant System
(ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System
(ISA) 0x000000B2 (178) Microsoft ACPI-Compliant System
(ISA) 0x000000B3 (179) Microsoft ACPI-Compliant System
(ISA) 0x000000B4 (180) Microsoft ACPI-Compliant System
(ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
(ISA) 0x000000B6 (182) Microsoft ACPI-Compliant System
(ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
(ISA) 0x000000B8 (184) Microsoft ACPI-Compliant System
(ISA) 0x000000B9 (185) Microsoft ACPI-Compliant System
(ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
(ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
(ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
(ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
(ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
(PCI) 0x00000010 (16) High Definition Audio Controller
(PCI) 0x00000010 (16) PCI standard PCI-to-PCI bridge
(PCI) 0x00000011 (17) PCI standard PCI-to-PCI bridge
(PCI) 0x00000011 (17) Standard Enhanced PCI to USB Host Controller
(PCI) 0x00000011 (17) Standard Enhanced PCI to USB Host Controller
(PCI) 0x00000011 (17) Standard Enhanced PCI to USB Host Controller
(PCI) 0x00000012 (18) Standard OpenHCD USB Host Controller
(PCI) 0x00000012 (18) Standard OpenHCD USB Host Controller
(PCI) 0x00000012 (18) Standard OpenHCD USB Host Controller
(PCI) 0x00000013 (19) AMD SATA Controller
(PCI) 0x00000013 (19) High Definition Audio Controller
(PCI) 0xFFFFFFFC (-4) Texas Instruments XHCI Controller
(PCI) 0xFFFFFFFD (-3) Intel(R) 82583V Gigabit Network Connection
(PCI) 0xFFFFFFFE (-2) AMD Radeon HD 6320 Graphics

6.3 Memory Map

The memory map of DRAM for the CT-CA56X with CT-BT601 carrier board under Windows® 7 Ultimate/64bit are shown below.

Memory

[00000000000A0000 - 00000000000BFFFF] AMD Radeon HD 6320 Graphics
[00000000000A0000 - 00000000000BFFFF] PCI bus
[00000000000C0000 - 00000000000DFFFF] PCI bus
[0000000067000000 - 000000007EFFFFFF] Motherboard resources
[000000007F000000 - 00000000FFFFFFFF] PCI bus
[00000000D0000000 - 00000000DFFFFFFF] AMD Radeon HD 6320 Graphics
[00000000E0000000 - 00000000EFFFFFFF] System board
[00000000FE900000 - 00000000FE90FFFF] Texas Instruments XHCI Controller
[00000000FE900000 - 00000000FE9FFFFF] PCI standard PCI-to-PCI bridge
[00000000FE910000 - 00000000FE911FFF] Texas Instruments XHCI Controller
[00000000FEA00000 - 00000000FEA1FFFF] Intel(R) 82583V Gigabit Network Connection
[00000000FEA00000 - 00000000FEAFFFFF] PCI standard PCI-to-PCI bridge
[00000000FEA20000 - 00000000FEA3FFFF] Intel(R) 82583V Gigabit Network Connection
[00000000FEA40000 - 00000000FEA43FFF] Intel(R) 82583V Gigabit Network Connection
[00000000FEB00000 - 00000000FEB3FFFF] AMD Radeon HD 6320 Graphics
[00000000FEB40000 - 00000000FEB43FFF] High Definition Audio Controller
[00000000FEB44000 - 00000000FEB47FFF] High Definition Audio Controller
[00000000FEB48000 - 00000000FEB480FF] Standard Enhanced PCI to USB Host Controller
[00000000FEB49000 - 00000000FEB49FFF] Standard OpenHCD USB Host Controller
[00000000FEB4A000 - 00000000FEB4AFFF] Standard OpenHCD USB Host Controller
[00000000FEB4B000 - 00000000FEB4B0FF] Standard Enhanced PCI to USB Host Controller
[00000000FEB4C000 - 00000000FEB4CFFF] Standard OpenHCD USB Host Controller
[00000000FEB4D000 - 00000000FEB4D0FF] Standard Enhanced PCI to USB Host Controller
[00000000FEB4E000 - 00000000FEB4EFFF] Standard OpenHCD USB Host Controller
[00000000FEB4F000 - 00000000FEB4F3FF] AMD SATA Controller
[00000000FEC00000 - 00000000FEC00FFF] Motherboard resources
[00000000FEC10000 - 00000000FEC10FFF] Motherboard resources
[00000000FED00000 - 00000000FED003FF] High precision event timer
[00000000FED00000 - 00000000FED00FFF] Motherboard resources
[00000000FED61000 - 00000000FED70FFF] Motherboard resources
[00000000FED80000 - 00000000FED8FFFF] Motherboard resources
[00000000FEE00000 - 00000000FEE00FFF] Motherboard resources
[00000000FFC00000 - 00000000FFFFFFFF] Motherboard resources

VII. Electrical Specification

7.1 Input Power

The carrier board for the CT-CA56X shall supply a single main power rail with a nominal value of +12V and two additional rails, a +5V standby power and +3V RTC power.