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C&T SOLUTION INC.

# USER'S MANUAL

## CE-ABT01

Intel® Atom™ E3800 COM Express Mini Size Type 10 Module

Version 100
March 11, 2016

# Table of Contents

**Prefaces** ..... **04**
Revision History ..... 04
Disclaimer ..... 04
Copyright Notice ..... 04
Trademarks Acknowledgement ..... 04
Environmental Protection Announcement ..... 04
Safety Precautions ..... 05

**Chapter 1 Introductions** ..... 06
1.1 Overview ..... 07
1.1.1 Key Features ..... 07
1.2 Hardware Specification ..... 08
1.3 Block Diagram ..... 09

**Chapter 2 Mechanical Specifications** ..... 10
2.1 Dimensions ..... 11
2.2 Board Layout ..... 12
2.3 Onboard Connectors ..... 13
2.3.1 XDP Debug Connector (CN4) ..... 13
2.3.2 CPLD JTAG Connector (CN2) ..... 13
2.4 COM Express Connectors ..... 14

**Chapter 3 Thermal Solutions** ..... 15
3.1 Heat Sink ..... 16
3.1.1 Dimensions ..... 16
3.1.2 Installation ..... 17

**Chapter 4 Features & Interfaces** ..... 18
4.1 Processor ..... 19
4.2 BIOS ..... 19
4.3 System Memory ..... 19
4.4 Graphics ..... 19
4.4.1 Analog Display Port ..... 20
4.4.2 LVDS ..... 20
4.4.3 Digital Display Interfaces (DDI) ..... 21
4.5 USB ..... 23
4.5.1 USB 2.0 ..... 23
4.5.2 USB 3.0 ..... 23
4.6 Ethernet ..... 24
4.7 SATA ..... 24
4.8 PCI Express ..... 24
4.9 Audio ..... 25
4.10 LPC ..... 25
4.11 SPI ..... 25
4.12 UART ..... 26
4.13 SMBus ..... 26
4.14 ExpressCard ..... 26
4.15 General Purpose Input Output ..... 27
4.15.1 GPIO Configuration ..... 27
4.15.2 Register Description ..... 27
4.15.3 Psuedo Code ..... 28

4.16 Power and System Management Signals ..... 29
4.17 Thermal Management Signals ..... 30
4.18 Miscellaneous Signals ..... 30
4.19 Watchdog Timer ..... 31
4.19.1 Board Design ..... 31
4.19.2 Psuedo Code ..... 31

**Chapter 5 Driver Installation** ..... 32

**Chapter 6 System BIOS** ..... 34
6.1 Advanced ..... 35
6.1.1 ACPI Settings ..... 36
6.1.2 F81801 Super IO Configuration ..... 36
6.1.3 Hardware Monitor ..... 37
6.1.4 W83627DHG Super IO Configuration ..... 38
6.1.5 W83627DHG Hardware Monitor1 ..... 39
6.1.6 Serial Port Console Redirection ..... 40
6.1.7 CPU Configuration ..... 41
6.1.8 SATA Configuration ..... 42
6.1.9 Miscellaneous Configuration ..... 42
6.1.10 LPSS & SCC Configuration ..... 43
6.1.11 Network Stack Configuration ..... 43
6.1.12 CSM Configuration ..... 44
6.1.13 USB Configuration ..... 45
6.1.14 Security Configuration ..... 46
6.2 Chipset ..... 47
6.2.1 Northbridge Configuration ..... 47
6.2.2 Southbridge Configuration ..... 50
6.3 Security ..... 52
6.3.1 Secure Boot Menu ..... 52
6.4 Boot ..... 53
6.5 Save and Exit ..... 54

# Prefaces

## Revision History

| Revision | Description | Date |
|---|---|---|
| 100 | Initial release | 2016/03/11 |

## Disclaimer

All specifications and information in this User's Manual are believed to be accurate and up to date. C&T Solution Inc. does not guarantee that the contents herein are complete, true, accurate or non-misleading. The information in this document is subject to change without notice and does not represent a commitment on the part of C&T Solution Inc.
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## Environmental Protection Announcement

Do not dispose this electronic device into the trash while discarding. Please recycle to minimize pollution and ensure environment protection.

# Safety Precautions

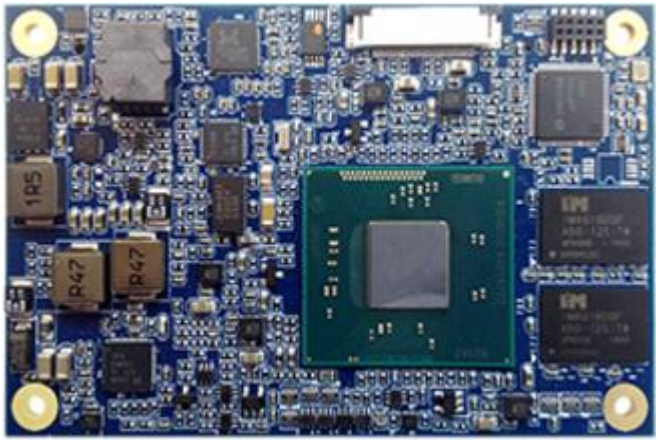
Before installing and using the equipment, please read the following precautions:

- Put this equipment on a reliable surface during installation. Dropping it or letting it fall could cause damage.
- The power outlet shall be installed near the equipment and shall be easily accessible.
- Turn off the system power and disconnect the power cord from its source before making any installation. Be sure both the system and the external devices are turned OFF. Sudden surge
- of power could ruin sensitive components. Make sure the equipment is properly grounded.
- When the power is connected, never open the equipment. The equipment should be opened only by qualified service personnel.
- Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
- Disconnect this equipment from the power before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
- Avoid the dusty, humidity and temperature extremes.
- Do not place heavy objects on the equipment.
- If the equipment is not used for long time, disconnect it from the power to avoid being damaged by transient over-voltage.
- The storage temperature shall be above -20°C and below 80°C.
- The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.
- If one of the following situation arises, get the equipment checked be service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well or it cannot work according the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.

Chapter 1

# Introductions

# 1. Introduction



## 1.1 Overview

The CE-ABT01 is a COM Express® form factor module in Mini Size with Type 10 pinout and features the Intel® Atom™ Processor E3800 Series (codename "Bay Trail") in FCBGA1170 package on 22nm process technology in a single chip solution. DDR3L memory is soldered down on-board with 2GB or 4GB as two different capacity options. The Intel HD graphics controller integrated within the processor supports two independent displays (from VGA, DDI, or LVDS).

The CE-ABT01 is based on the COM Express® specification and features a standardized connector layout that carries a specified set of signals. The Type 10 pin-out connectors support DDI/LVDS/VGA, SATA, HD audio, Gigabit Ethernet, PCIe and USB 3.0. This computer-on-module provides the core system functions and requires a carrier board to bring out I/O to form a complete system. To accommodate a variety of OEM/ODM requirements, the COM Express module with a carrier board is the best cost-effective solution and reduces development time.

### 1.1.1 Key Features

- Intel® Atom™ Processor E3845, 1.91GHz / E3827, 1.75GHz/ E3815, 1.46GHz or Intel ® Celeron® J1900, 2.0GHz Processor
- DDR3L onboard memory support up to 2GB / 4GB
- 1x DDI, 1x 1-ch 24-bit LVDS, 1x VGA
- Supports 3x PCIe x1
- Supports 2x SATA 3.0Gb/s
- Onboard eMMC Flash 16GB / 32GB (Optional)
- Supports 1x USB 3.0, 8x USB 2.0
- 1x 8-bit GPIO (4-in / 4-out)
- Supports TPM 1.2
- 5 to 19V wide range power input supporting AT/ATX mode
- -40°C to 85°C extended operating temperature

## 1.2 Hardware Specification

### CPU
- Intel® Atom™ Processor E3800 Series, FCBGA1170 package
  - Atom™ E3845: 4-core, 1.91GHz, TDP 10W
  - Atom™ E3827: 2-core, 1.75GHz. TDP 8W
  - Atom™ E3815: 1-core, 1.46GHz, TDP 5W
  - Celeron® J1900: 4-core, 2.00GHz, TDP 10W

### System Memory
- 2GB/4GB DDR3L memory down
- non-ECC unbuffered
- Data transfer rates up to 1333MT/s

### BIOS
- AMI uEFI BIOS
- 8MB SPI flash ROM

### TPM
- TPM 1.2 support

### Graphics
- Intel® HD Graphics Gen 7 integrated in CPU
- 1x VGA, resolution up to 2560x1600@60Hz
- 1x DDI interfaces
  - 1st DDI port reserved for DP/eDP/HDMI/DVI
- eDP to LVDS
  - Realtek RTD2136R
  - 2-channel 24-bit LVDS

### Ethernet
- One Intel® I210AT GbE Controller
- 10/100/1000BASE-TX Ethernet
- Wake-On-LAN/PXE support

### USB
- SMSC 4604C USB2.0 HSIC host controller
- 4x USB 2.0 ports

### Audio
- Integrated in Bay Trail SOC
- HD audio codec

### Storage
- eMMC onboard (optional 16GB or 32GB)

### COM Express Type 10 Row A/B I/O
- 1x 1-ch 24-bit LVDS
- 1x VGA
- 2x SATA II port
- 1x USB3.0 port
- 8x USB2.0 port
- 1x DDI port
- 1x HD audio interface
- 1x LPC interface
- 1x GbE
- 3x PCIe x1 port
- 2x UART port
- 1x SMBus
- 1x SPI interface
- 1x I2C interface
- 1x 4-bit GPI
- 1x 4-bit GPO
- 2x Fan control signals
- 1x Reset signal
- 1x Power-on button signal
- 1x Watchdog Timer

### Watchdog Timer
- H/W Reset, 1-255 steps
- 1 sec. or 1min. Increments

### Hardware Monitor
- CPU core/IO power
- Memory power

### Debug
- 1x 60-pin XDP connector

### Form Factor
- COM Express Type 10, Mini Size, 84mm x 55mm

### Power
- AT/ATX mode supported
- AT mode:
  - Vin: +5V to +19V
- ATX mode:
  - Vin: +5V to +19V
  - Vstandby: +5VSB
- ACPI 5.0 compliant

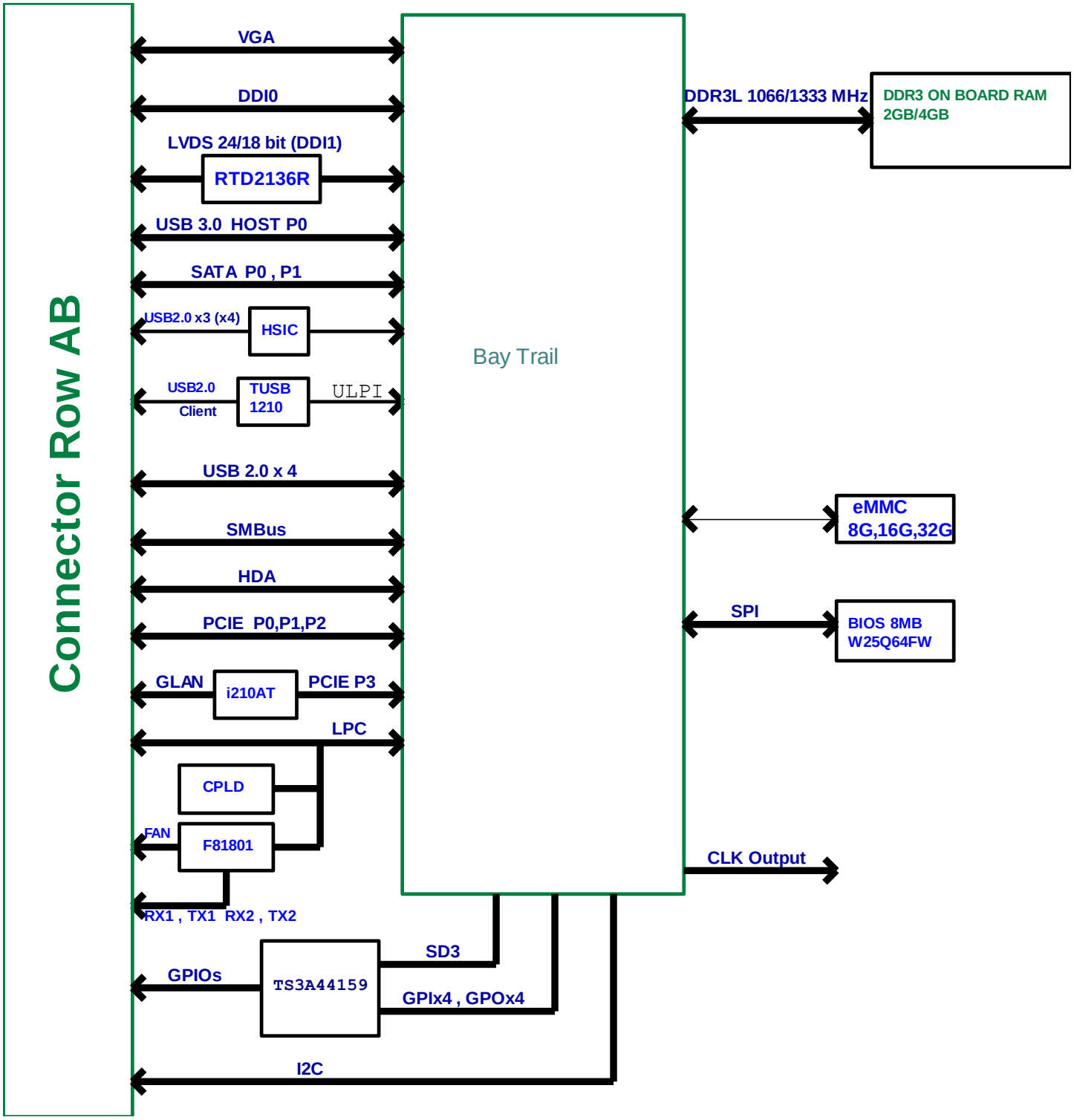
### Operating Temp.
- CE-ABT01: 0°C ~ 60°C
- CE-ABT01r: -20°C ~ 70°C
- CE-ABT01e: -40°C ~ 85°C

### Storage Temp.
- -40°C to 85°C

### Operating Humidity
- 10% to 90% relative humidity, non-condensing

### Certifications
- CE
- FCC Class A

## 1.3 Block Diagram



Chapter 2

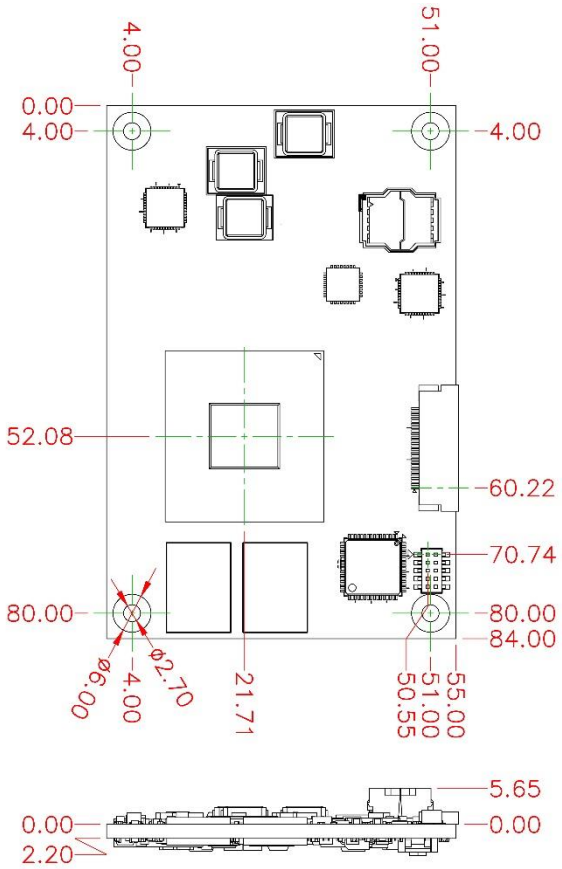
# Mechanical Specifications

# 2. Mechanical Specifications

The CE-ABT01 is a 84mm x 55mm COM Express Mini Size module. The mounting holes shown in the drawing below are for stacking the module with a heat spreader or heat sink and carrier board. The mounting holes are 2.7mm in diameter, and 2.5mm thick mounting hardware shall be used.

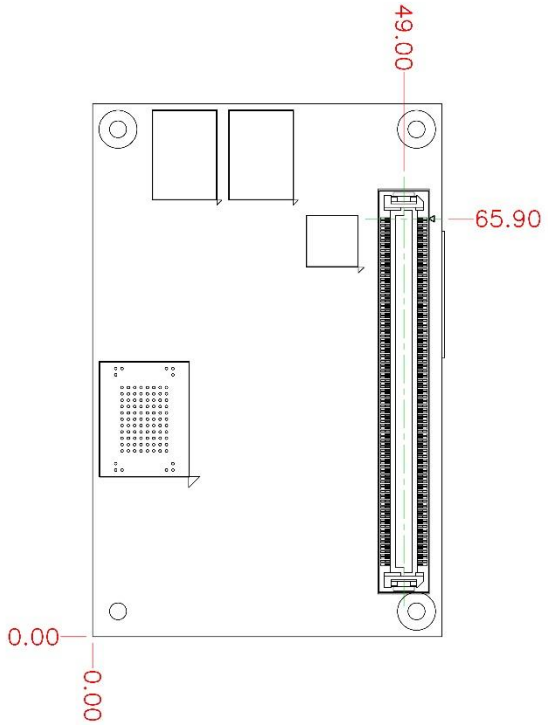
## 2.1 Dimensions

**Top View**




**Units: mm**

**Bottom View**

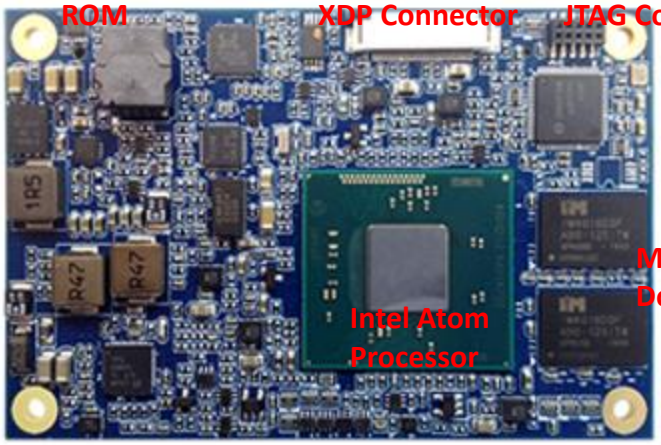



**Units: mm**

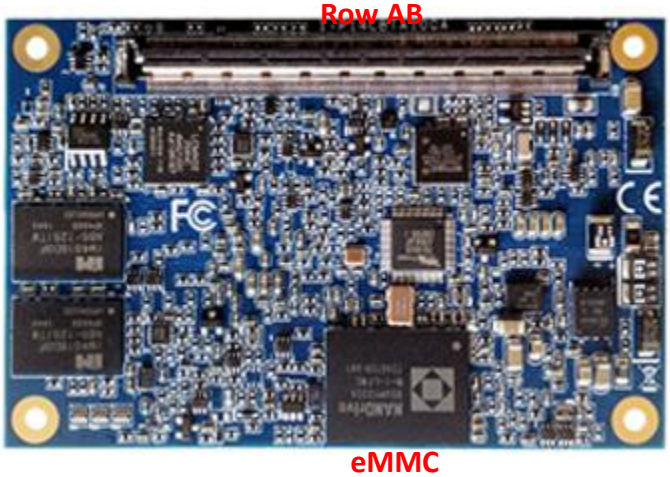
## 2.2 Board Layout

CPU, XDP connector, JTAG connector are mounted on top side of the module. COM Express AB connector is mounted on the bottom side of the module.

**Top View**



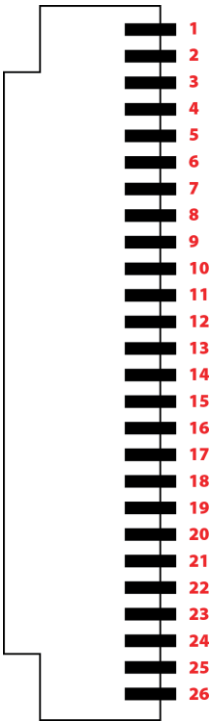

**Bottom View**



## 2.3 Onboard Connectors

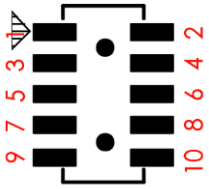
### 2.3.1 XDP Debug Connector (CN4)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | PREQ | 14 | NC |
| 2 | PRDY | 15 | NC |
| 3 | GND | 16 | 1.8V |
| 4 | GPIO_S5_23 | 17 | PLTRST# |
| 5 | GPIO_S5_24 | 18 | SYSRST# |
| 6 | GND | 19 | GND |
| 7 | GPIO_S5_25 | 20 | TDO |
| 8 | GPIO_S5_26 | 21 | TRST# |
| 9 | GND | 22 | TDI |
| 10 | RSMRST# | 23 | TMS |
| 11 | PWRBTN# | 24 | NC |
| 12 | PWROK | 25 | GND |
| 13 | RTCRST# | 26 | TCK |




### 2.3.2 CPLD JTAG Connector (CN2)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +3.3V | 2 | GND |
| 3 | TDO | 4 | GND |
| 5 | TDI | 6 | GND |
| 7 | TMS | 8 | GND |
| 9 | TCK | 10 | GND |



## 2.4 COM Express Connectors

The CE-ABT01 is connected to the carrier board via one 220-pin connector. The connector contains two rows of signals. Their pinouts are as shown in the table below.

| Pin | Row A | Row B |
|---|---|---|
| 1 | GND | GND |
| 2 | GBE0_MDI3- | GBE0_ACT# |
| 3 | GBE0_MDI3+ | LPC_FRAME# |
| 4 | GBE0_LINK100# | LPC_AD0 |
| 5 | GBE0_LINK1000# | LPC_AD1 |
| 6 | GBE0_MDI2- | LPC_AD2 |
| 7 | GBE0_MDI2+ | LPC_AD3 |
| 8 | GBE0_LINK# | LPC_DRQ0# |
| 9 | GBE0_MDI1- | LPC_DRQ1# |
| 10 | GBE0_MDI1+ | LPC_CLK |
| 11 | GND | GND |
| 12 | GBE0_MDI0- | PWRBTN#- |
| 13 | GBE0_MDI0+ | SMB_CK |
| 14 | GBE0_CTREF | SMB_DAT |
| 15 | SUS_S3# | SMB_ALERT# |
| 16 | SATA0_TX+ | SATA1_TX+ |
| 17 | SATA0_TX- | SATA1_TX- |
| 18 | SUS_S4# | SUS_STAT# |
| 19 | SATA0_RX+ | SATA1_RX+ |
| 20 | SATA0_RX- | SATA1_RX- |
| 21 | GND | GND |
| 22 | USB_SSRX0- | USB_SSTX0- |
| 23 | USB_SSRX0+ | USB_SSTX0+ |
| 24 | SUS_S5# | PWR_OK |
| 25 | NC | NC |
| 26 | NC | NC |
| 27 | BATLOW# | WDT |
| 28 | (S)ATA_ACT# | NC |
| 29 | AC/HDA_SYNC | AC/HAD_SDIN1 |
| 30 | AC/HAD_RST# | AC/HAD_SDIN0 |
| 31 | GND | GND |
| 32 | AC/HDA_BITCLK | SPKR |
| 33 | AC/HAD_SDOUT | I2C_CK |
| 34 | BIOS_DIS0# | I2C_DAT |
| 35 | THRMTRIP# | THRM# |
| 36 | USB6- | USB7- |
| 37 | USB6+ | USB7+ |
| 38 | USB_6_7_OC# | USB_4_5_OC# |
| 39 | USB4- | USB5- |
| 40 | USB4+ | USB5+ |
| 41 | GND | GND |
| 42 | USB2- | USB3- |
| 43 | USB2+ | USB3+ |
| 44 | USB_2_3_OC# | USB_0_1_OC# |
| 45 | USB0- | USB1- |
| 46 | USB0+ | USB1+ |
| 47 | VCC_RTC | EXCD1_PERST# |
| 48 | EXCD0_PERST# | EXCD1_CPPE# |
| 49 | EXCD0_CPPE# | SYS_RESET# |
| 50 | LPC_SERIRQ | CB_RESET# |
| 51 | GND | GND |
| 52 | *CRT_RED(C&T) | *CRT_GREEN(C&T) |
| 53 | *VSD3(C&T) | *CRT_BLUE(C&T) |
| 54 | GPI0 | GPO1 |
| 55 | *CRT_DDC_CLK(C&T) | *CRT_HSYNC(C&T) |

| Pin | Row A | Row B |
|---|---|---|
| 56 | *CRT_DDC_DATA(C&T) | *CRT_VSYNC(C&T) |
| 57 | GND | GPO2 |
| 58 | NC | NC |
| 59 | NC | NC |
| 60 | GND | GND |
| 61 | PCIE2_TX+ | PCIE2_RX+ |
| 62 | PCIE2_TX- | PCIE2_RX- |
| 63 | GPI1 | GPO3 |
| 64 | PCIE1_TX+ | PCIE1_RX+ |
| 65 | PCIE1_TX- | PCIE1_RX- |
| 66 | GND | WAKE0# |
| 67 | GPI2 | WAKE1# |
| 68 | PCIE0_TX+ | PCIE0_RX+ |
| 69 | PCIE0_TX- | PCIE0_RX- |
| 70 | GND | GND |
| 71 | LVDS_A0+ | DDI0_PAIR0+ |
| 72 | LVDS_A0- | DDI0_PAIR0- |
| 73 | LVDS_A1+ | DDI0_PAIR1+ |
| 74 | LVDS_A1- | DDI0_PAIR1- |
| 75 | LVDS_A2+ | DDI0_PAIR2+ |
| 76 | LVDS_A2- | DDI0_PAIR2- |
| 77 | LVDS_VDD_EN | NC |
| 78 | LVDS_A3+ | NC |
| 79 | LVDS_A3- | LVDS_BKLT_EN |
| 80 | GND | GND |
| 81 | LVDS_A_CK+ | DDI0_PAIR3+ |
| 82 | LVDS_A_CK- | DDI0_PAIR3- |
| 83 | LVDS_I2C_CK | LVDS_BKLT_CTRL |
| 84 | LVDS_I2C_DAT | VCC_5V_SBY |
| 85 | GPI3 | VCC_5V_SBY |
| 86 | *SD_PWR_EN_L(C&T) | VCC_5V_SBY |
| 87 | NC | VCC_5V_SBY |
| 88 | PCIE_CK_REF0+ | BIOS_DIS1# |
| 89 | PCIE_CK_REF0- | DDI0_HPD |
| 90 | GND | GND |
| 91 | SPI_POWER | NC |
| 92 | SPI_MISO | NC |
| 93 | GPO0 | NC |
| 94 | SPI_CLK | NC |
| 95 | SPI_MOSI | DDI0_DDC_AUX_SEL |
| 96 | NC | NC |
| 97 | TYPE10# | SPI_CS# |
| 98 | SER0_TX | DDI0_CTRLCLK_AUX+ |
| 99 | SER0_RX | DDI0_CTRLCLK_AUX- |
| 100 | GND | GND |
| 101 | SER1_TX | FAN_PWMOUT |
| 102 | SER1_RX | FAN_TACHIN |
| 103 | LID# | SLEEP# |
| 104 | VCC_12V | VCC_12V |
| 105 | VCC_12V | VCC_12V |
| 106 | VCC_12V | VCC_12V |
| 107 | VCC_12V | VCC_12V |
| 108 | VCC_12V | VCC_12V |
| 109 | VCC_12V | VCC_12V |
| 110 | GND | GND |

Chapter 3

# Thermal Solutions

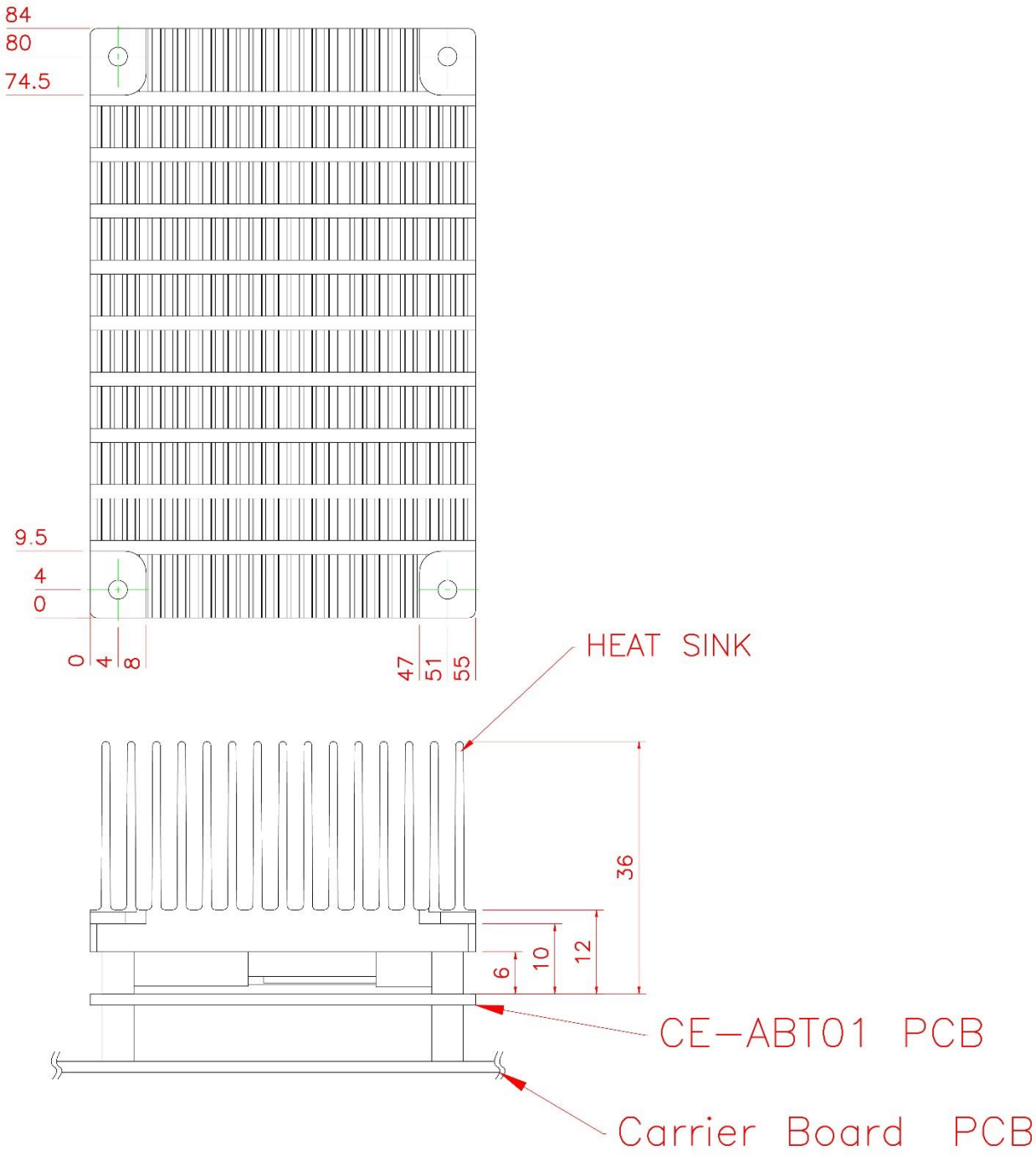
# 3. Mechanical Specifications

Heat sink can be used as the thermal solutions for the CE-ABT01 COM Express Module to dissipate heat. Its mechanical dimension and assembly procedure is described in this section.

## 3.1 Heat Sink

### 3.1.1 Dimensions

**Units: mm**

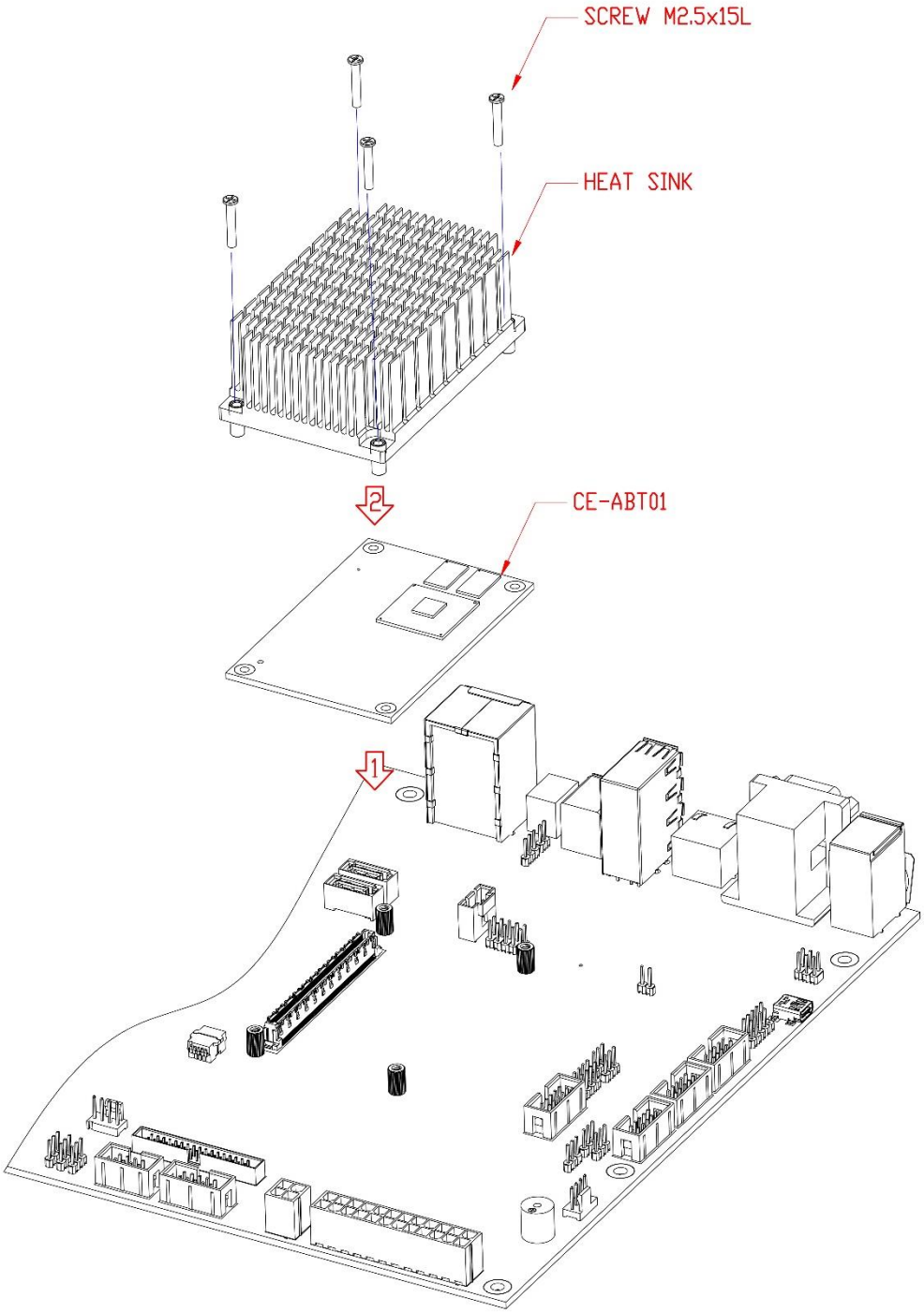


### 3.1.2 Installation

**Step 1:** Align the COM Express connectors on the module with the corresponding connectors on the carrier board. Make sure the four holes at the corners of the module line up with the corresponding standoffs on the carrier board. Press down on the module until it is properly seated on the carrier board.

**Step 2:** Place the fan sink on top of the module.

**Step 3:** Use four screws (M2.5x15L) to secure the fan sink to the carrier board through the corresponding holes on the module.



Chapter 4

# Features & Interfaces

# 4. Features & Interfaces

## 4.1 Processor

The CE-ABT01 supports the Intel® Atom™ processor E3800 Series which utilizes 22nm process technology with 3-D Tri-Gate transistors to deliver significant improvement in computational performance and energy-efficiency. Based on a new micro-architecture, the processor is designed for a one-chip platform. This system-on-chip (SoC) solution platform brings enhanced graphics, greater performance, lower cost, easier validation, and improved x-y footprint to a broad range of intelligent systems. The processor includes an Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

## 4.2 BIOS

AMI uEFI BIOS on 8MB SPI Flash ROM is used on the CE-ABT01.

## 4.3 System Memory

The Integrated Memory Controller (IMC) of the processor supports dual channel, non-ECC, unbuffered DDR3L-1333 memory up to 8GB with data transfer rates up to 1333MT/s.

## 4.4 Graphics

The graphics is integrated in the processor and based on Intel® HD Graphics Gen 7, enabling substantial gains in performance and lower power consumption.

- DirectX 11 support
- OpenGL 4.0 support
- Graphics Base Frequency: 542 MHz
- Graphics Max Dynamic Frequency: 792 MHz
- Full HD video playback
- Maximum resolution of 2560x1600@60Hz

Graphics outputs are as follows:

- DDI port: DisplayPort 1.2, 2560x1600@60Hz; HDMI 1.4,1080p@60Hz
- VGA: 1600x1200@60Hz (SKU dependent)
- LVDS: 2048x1536

### 4.4.1 Analog Display Port

The VGA port is used for boot, safe mode, legacy games, etc. It can be changed by an application without OS/driver notification, due to legacy requirements.

| Signal | I/O | Description |
|---|---|---|
| VGA_RED | O | Red Analog Video Output: This signal is a VGA Analog video output from the internal color palette DAC. |
| VGA_GREEN | O | Green Analog Video Output: This signal is a VGA Analog video output from the internal color palette DAC. |
| VGA_BLUE | O | Blue Analog Video Output: This signal is a VGA Analog video output from the internal color palette DAC. |
| VGA_HSYNC | O | VGA Horizontal Synchronization: This signal is used as the horizontal sync (polarity is programmable) or "sync interval". |
| VGA_VSYNC | O | VGA Vertical Synchronization: This signal is used as the horizontal sync (polarity is programmable) or "sync interval". |
| VGA_I2C_CLK | I/O | VGA DDC Clock: EDID support for an external VGA display. |
| VGA_I2C_DATA | I/O | VGA DDC Data: EDID support for an external VGA display. |

### 4.4.2 LVDS

Each of the two LVDS transmitter channels consist of 4 data pairs and a clock pair. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals.

| Signal | I/O | Description |
|---|---|---|
| LVDS_A/B[3:0]+ | O | Differential data output |
| LVDS_A/B[3:0]- | O | Differential data output |
| LVDS_A/B_CLK+ | O | Differential clock output - positive |
| LVDS_A/B_CLK- | O | Differential clock output - negative |
| LVDS_VDD_EN | O | LVDS panel power enable |
| LVDS_BKLT_EN | O | Panel backlight enable control |
| LVDS_BKLT_CTR | O | Panel backlight brightness control |
| LVDS_I2C_CLK | I/O | LVDS flat panel I2C clock for EDID read and control. |
| LVDS_I2C_DATA | I/O | LVDS flat panel I2C data for EDID read and control. |

### 4.4.3 Digital Display Interfaces (DDI)

The processor supports one Digital Display Interfaces that can be configured as DisplayPort, HDMI or DVI.

| Signal | I/O | Description |
|---|---|---|
| DDI[1:2]_PAIR[0:3]+<br>DDI[1:2]_PAIR[0:3]- | O | DDI 1 to 2 Pair[0:3] differential pairs |
| DDI[1:2]_DDC_AUX_SEL | I | Selects the function of DDI[1:2]_CTRLCLK_AUX+ and DDI[1:2]_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CTRLCLK and CTRLDATA signals. |
| DDI[1:2]_CTRLCLK_AUX+ | I/O | DP AUX+ function if DDI[1:2]_DDC_AUX_SEL is no connect |
| | I/O | HDMI/DVI I2C CTRLCLK if DDI[1:2]_DDC_AUX_SEL is pulled high |
| DDI[1:2]_CTRLDATA_AUX- | I/O | DP AUX- function if DDI[1:2]_DDC_AUX_SEL is not connected |
| | I/O | HDMI/DVI I2C CTRLDATA if DDI[1:2]_DDC_AUX_SEL is pulled high |
| DDI[1:2]_HPD | I | DDI Hot-Plug Detect |

**DDI Pin Definitions**

| | Signal | Pin | eDP/DP | HDMI/DVI |
|---|---|---|---|---|
| DDI0 | DDI0_PAIR0+ | B71 | DP1_LANE0+ | TMDS1_DATA2+ |
| | DDI0_PAIR0- | B72 | DP1_LANE0- | TMDS1_DATA2- |
| | DDI0_PAIR1+ | B73 | DP1_LANE1+ | TMDS1_DATA1+ |
| | DDI0_PAIR1- | B74 | DP1_LANE1- | TMDS1_DATA1- |
| | DDI0_PAIR2+ | B75 | DP1_LANE2+ | TMDS1_DATA0+ |
| | DDI0_PAIR2- | B76 | DP1_LANE2- | TMDS1_DATA0- |
| | DDI0_PAIR3+ | B81 | DP1_LANE3+ | TMDS1_CLK+ |
| | DDI0_PAIR3- | B82 | DP1_LANE3- | TMDS1_CLK- |
| | DDI0_CTRLCLK_AUX+ | B98 | DP1_AUX+ | TMDS1_SCL |
| | DDI0_CTRLDATA_AUX- | B99 | DP1_AUX- | TMDS1_SDA |
| | DDI0_DDC_AUX_SEL | B95 | CONFIG1<br>(pull down to GND) | Pull up to 5V |
| | DDI0_HPD (3.3V active high signal) | B89 | | |

#### 4.4.3.1 High Definition Multimedia Interface (HDMI)

The HDMI port is provided for transmitting uncompressed digital audio and video signals to television sets, projectors and other video displays.

#### 4.4.3.2 Digital Video Interface (DVI)

The DDI ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver, which is similar to the HDMI protocol but the audio and CEC. When a system has support for DVI-I port, then either VGA or the DVI-D through a single DVI-I connector can be driven but not both simultaneously.

| HDMI Signal | I/O | Description |
|---|---|---|
| TMDS[1:2]_CLK+<br>TMDS[1:2]_CLK- | O | HDMI/DVI TMDS Clock differential pair |
| TMDS[1:2]_DATA[0:2]+<br>TMDS[1:2]_DATA[0:2]- | O | HDMI/DVI TMDS lanes 0, 1 and 2 differential pairs |
| HDMI[1:2]_SCL | I/O | HDMI/DVI I2C control clock |
| HDMI[1:2]_SDA | I/O | HDMI/DVI I2C control data |

#### 4.4.3.3 Display Port (DP)

The DisplayPort output is a digital communication interface that utilized differential signaling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

## 4.5 USB

The Intel® SOC USB Host Controller (xHCI,EHCI) supports:

- One super speed (SS) port on xHCI,
- Four Full Speed(FS)/High Speed(HS) ports on xHCI or EHCI.
- Two High Speed (HS) High Speed Inter-Chip (HSIC) ports on xHCI.

The SMSC 4604C USB 2.0 HSIC Host Controller supports an additional 3 USB 2.0 ports.

### 4.5.1 USB 2.0

Each USB 2.0 port supports USB 1.1 and 2.0 compliant devices.

| Signal | I/O | Description |
|---|---|---|
| USB[0:7]+<br>USB[0:7]- | I/O | USB differential pairs, channels 0 through 7 |
| USB_0_1_OC# | I | USB over-current sense, USB 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. |
| USB_2_3_OC# | I | USB over-current sense, USB 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. |
| USB_4_5_OC# | I | USB over-current sense, USB 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. |
| USB_6_7_OC# | I | USB over-current sense, USB 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. |

### 4.5.2 USB 3.0

| Signal | I/O | Description |
|---|---|---|
| USB_SSRX[0:3]+<br>USB_SSRX[0:3]- | I | USB differential pairs, channels 0 through 3, receive Data/Address/Command signals |
| USB_SSTX[0:3]+<br>USB_SSTX[0:3]- | O | USB differential pairs, channels 0 through 3, transmit Data/Address/Command signals |

## 4.6 Ethernet

The CE-ABT01 features an Intel® I210 AT Ethernet Controller, which is connected to one PCIe x1, and provides a 10/100/1000Mb/s interface.

| Signal | I/O | Description |
|---|---|---|
| GBE0_MDI[0:3]+<br>GBE0_MDI[0:3]- | I/O | Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100 and 10 Mbit/sec modes. Some pairs are unused in some modes, per the following:<br>1000BASE-T 100BASE-TX 10BASE-T<br>MDI[0]+/- B1_DA+/- TX+/- TX+/-<br>MDI[1]+/- B1_DB+/- RX+/- RX+/-<br>MDI[2]+/- B1_DC+/-<br>MDI[3]+/- B1_DD+/- |
| GBE0_ACT# | OD | Gigabit Ethernet Controller 0 activity indicator, active low |
| GBE0_LINK# | OD | Gigabit Ethernet Controller 0 link indicator, active low |
| GBE0_LINK100# | OD | Gigabit Ethernet Controller 0 100 Mbit/sec link indicator, active low |
| GBE0_LINK1000# | OD | Gigabit Ethernet Controller 0 1000 Mbit/sec link indicator, active low |
| GBE0_CTREF | REF | Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is 3.3V. |

## 4.7 SATA

The SOC has one integrated SATA host controller that supports independent DMA operation and data transfer rates of up to 3.0 Gb/s.

| Signal | I/O | Description |
|---|---|---|
| SATA[0..1]_TX+<br>SATA[0..1]_TX- | O | Serial ATA Port 0~1 transmit differential pair |
| SATA[0..1]_RX+<br>SATA[0..1]_RX- | I | Serial ATA Port 0~1 receive differential pair |
| (S)ATA_ACT# | OC | ATA (parallel and serial) activity indicator, active low |

## 4.8 PCI Express

There are four one-lane PCI Express ports provided by the SOC, but one of the ports is used for Ethernet. The ports are compliant to the PCI Express 2.0 specification running at 5 Gb/s.

| Signal | I/O | Description |
|---|---|---|
| PCIE[0:3]_TX+<br>PCIE[0:3]_TX- | O | PCI Express Differential transmit Pairs 0 through 6 |
| PCIE[0:3]_RX+<br>PCIE[0:3]_RX- | I | PCI Express Differential receive Pairs 0 through 6 |
| PCIE_CK_REF0+<br>PCIE_CK_REF0- | O | Reference clock output for all PCI Express and PCI Express Graphics lanes |

## 4.9 Audio

The processor also integrates dedicated an HD audio controller to drive audio on integrated digital display interfaces, such as HDMI and DisplayPort. The HD audio controller on the PCH would continue to support down codecs, and so on. The processor Mini HD audio controller supports two High Definition Audio streams simultaneously on any of the three digital ports.

| Signal | I/O | Description |
|---|---|---|
| AC/HDA_RST# | O | Reset output to CODEC, active low |
| AC/HDA_SYNC | O | Sample-synchronization signal to the CODEC(s) |
| AC/HDA_BITCLK | O | Serial data clock generated by the external CODEC(s) |
| AC/HDA_SDOUT | O | Serial TDM data output to the CODEC |
| AC/HDA_SDIN[2:0] | I/O | Serial TDM data input from up to 3 CODECs |

## 4.10 LPC

The LPC interface provides legacy I/O support on a carrier board via a Super I/O and system management devices.

| Signal | I/O | Description |
|---|---|---|
| LPC_AD[3:0] | I/O | LPC multiplexed address, command and data |
| LPC_FRAME# | O | LPC frame indicates the start of an LPC cycle |
| LPC_DRQ[0:1]# | I | LPC serial DMA request input |
| LPC_SERIRQ | I/O | LPC serial interrupt |
| LPC_CLK | O | LPC clock output – 33MHz nominal |

## 4.11 SPI

The Serial Peripheral Interface (SPI) is a 4-pin interface that supports SPI-compatible flash devices. The SPI flash device can be up to 8MB (64Mb).

| Signal | I/O | Description |
|---|---|---|
| SPI_CS# | O | Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1 |
| SPI_MISO | I | Data in to Module from Carrier SPI |
| SPI_MISI | O | Data out from Module to Carrier SPI |
| SPI_CLK | O | Clock from Module to Carrier SPI |
| SPI_POWER | O | Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100ma of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board. |

## 4.12 UART

The CE-ABT01 module supports two serial RX/TX ports.

| Signal | I/O | Description |
|---|---|---|
| SER[0:1]_TX | O | UART transmitter |
| SER[0:1]_RX | I | UART receiver |

## 4.13 SMBus

The SMBus port is specified for system management functions. It is used on the module to manage system function such as reading the DRAM SPD EEPROM and setting clock synthesizer parameters. If the SMBus is used on the carrier board, great care must be taken that no conflicts with the on-module SMBus devices occur. It may be useful for implementation of standards such as Smart Battery on the carrier board. The maximum capacitance on the carrier board shall not exceed 100pF.

| Signal | I/O | Description |
|---|---|---|
| SMB_CK | I/OD | System Management Bus bidirectional clock line |
| SMB_DAT | I/OD | System Management Bus bidirectional data line |
| SMB_ALERT# | I | System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. |

## 4.14 ExpressCard

ExpressCard is a small form factor expansion card that uses PCI Express or USB as the interface. It is similar in concept and scope to CardBus. The CE-ABT01 supports two Express Card interfaces.

| Signal | I/O | Description |
|---|---|---|
| EXCD[0:1]_CPPE# | I | PCI ExpressCard: PCI Express capable card request, active low, one per card |
| EXCD[0:1]_PERST# | O | PCI ExpressCard: reset, active low, one per card |

# 4.15 General Purpose Input Output

GPI and GPO pins may be implemented as GPIO. GPI and GPO pins may be implemented as SDIO.

| Signal | I/O | Description |
|---|---|---|
| GPO[0:3] | O | General purpose output pins. Upon a hardware reset, these outputs should be low. |
| GPI[0:3] | I | General purpose input pins. Pulled high internally on the Module. |

## 4.15.1 GPIO Configuration

The output pin default setting is HIGH.

| Pin # | GPIO # | Default Configuration |
|---|---|---|
| B63 | GPIO7 | **GPO3** |
| B57 | GPIO6 | **GPO2** |
| B54 | GPIO5 | **GPO1** |
| A93 | GPIO4 | **GPO0** |
| A85 | GPIO3 | **GPI3** |
| A67 | GPIO2 | **GPI2** |
| A63 | GPIO1 | **GPI1** |
| A54 | GPIO0 | **GPI0** |

The GPIO function, provided by the SOC can be accessed through GPIO Base Address Register (GPIOBASE). This address is at memory-mapped IOs. The configuration on CE-ABT01 is described as below.

| Register | Address |
|---|---|
| GPIOBASE Base Address | 0x1C00 |

The memory I/O read/write function is used to access and configure the GPIO. Through the memory I/O read or write command, the current status of GPIO can configure each pin to input or output.

## 4.15.2 Register Description

### 4.15.2.1 GPIO Use Select

■ GPIO Use Select Register 1

1. *(Offset **GPIOBASE+0x00**)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | GPIO0 | |

2. *(Offset **GPIOBASE+0x02**)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | GPIO4 | GPIO3 | | | | GPIO2 | GPIO1 |

■ GPIO Use Select Register 2

1. *(Offset **GPIOBASE+0x30**)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | | GPIO7 | GPIO6 | GPIO5 | | |

Note:
Bit X = 0 means Native Function
Bit X = 1 means GPIO Function

### 4.15.2.2 GPIO Input/Output Select

■ GPIO Input/Output Select Register 1

1. *(Offset **GPIOBASE+0x04**)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | GPIO0 | |

2. *(Offset **GPIOBASE+0x06**)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | GPIO4 | GPIO3 | | | | GPIO2 | GPIO1 |

■ GPIO Input/Output Select Register 2

1. (Offset GPIOBASE+0x34)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | | GPIO7 | GPIO6 | GPIO5 | | |

Note:
Bit X = 0 means Native Function
Bit X = 1 means GPIO Function

### 4.15.2.3 GPIO Level for Input or Output

If **Pin X** configures as **output** pin, you can decide its output value (0 or 1).
If it is programmed as an input, this register reflects the state of the input signal.

■ GPIO Level for Input or Output Register 1

1. *(Offset GPIOBASE+0x0C)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | GPIO0 | |

2. *(Offset GPIOBASE+0x0E)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | GPIO4 | GPIO3 | | | | GPIO2 | GPIO1 |

■ GPIO Level for Input or Output Register 2

1. *(Offset GPIOBASE+0x38)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | | GPIO7 | GPIO6 | GPIO5 | | |

#### 4.15.2.4 GPIO Signal Invert Register

It will invert the polarity of the Input Port register data.

1. *(Offset GPIOBASE+0x2C)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | GPIO0 | |

2. *(Offset GPIOBASE+0x2E)*

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| | GPIO4 | GPIO3 | | | | GPIO2 | GPIO1 |

Note:
Bit X = 0 means Polarity is retained
Bit X = 1 means Polarity is inverted
GPIO4~GPIO7 cannot be set to inverted.

### 4.15.3 Psuedo Code

***Example 1:*** Change GPIO2 from input to output

```
Step1: ByteData = ReadIOByte(0x506)        //Read current setting from configuration
                                           //Register
Step2: ByteData = ByteData | 0xFD          //Set Bit1 to 0. It means output
Step3: WriteIOByte(0x506, ByteData)        //Write back to configuration register
```

***Example 2:*** Set GPIO7 to output LOW

```
Step1: ByteData = ReadIOByte(0x538)        //Read current setting from Output Port
                                           //Register
Step2: ByteData =ByteData & 0xEF           //Set Bit4 to 0. It means output low
Step3: WriteIOByte(0x538, ByteData)        //Write back to Output Port Register
```

## 4.16 Power and System Management Signals

| Signal | I/O | Description |
|---|---|---|
| SUS_S3# | O | Indicates system is suspended to RAM state. Active low output. |
| SUS_S4# | O | Indicates system is suspended to Disk state. Active low output. |
| SUS_S5# | O | Indicates system is in Soft Off state. |
| SUS_STAT# | O | Indicates imminent suspend operation. |
| PWRBTN# | I | Power button to bring system out of S5 (soft off), active on rising edge. |
| PWR_OK | I | Power OK from main power supply |
| BATLOW# | I | Indicates that external battery is low. |
| SYS_RESET# | I | Reset button input. Active low input. |
| CB_RESET# | O | Carrier Board Reset. Active low input. |
| WAKE0# | I | PCI Express wake up signal. |
| WAKE1# | I | General purpose wake up signal. |
| VCC_RTC | I | RTC External Battery |
| LID# | I | LID switch |
| SLEEP# | I | Sleep Button |
| FAN_PWMOUT | O | FAN PWM out |
| FAN_TACHIN | I | Fan Tacho in |

## 4.17 Thermal Management Signals

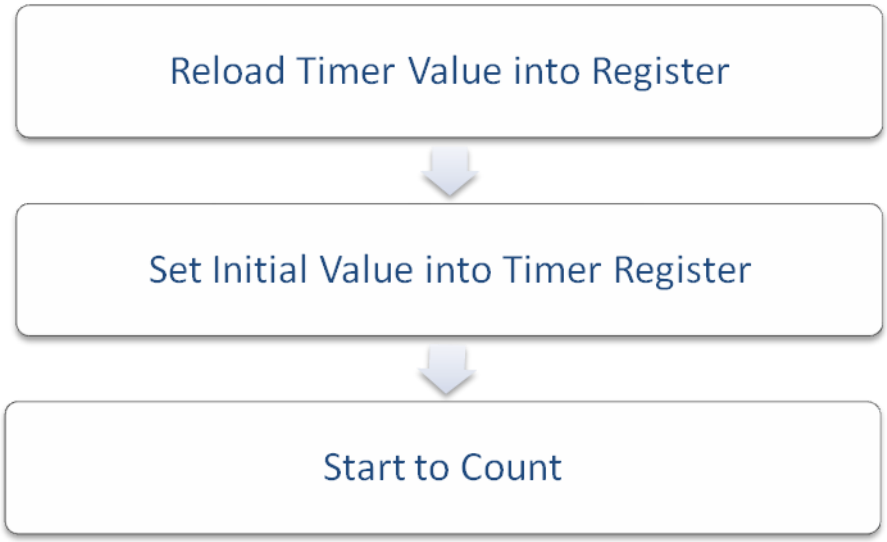
| Signal | I/O | Description |
|---|---|---|
| THRMTRIP# | O | Active low output indicating that the CPU has entered thermal shutdown. |
| THRM# | I | Input from off-module temp sensor indicating and over-temp situation. |

## 4.18 Miscellaneous Signals

| Signal | I/O | Description |
|---|---|---|
| I2C_CK | O | General purpose I2C port clock output |
| I2C_DAT | I/O | General purpose I2C port data I/O lin |
| WDT | O | Indicator for Watchdog Timeout |
| SPKR | O | Output for audio enunciator-the "speaker" in PC-AT systems |
| BIOS_DIS0#<br>BIOS_DIS1# | I | Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to the table below for strapping option of BIOS disable signals. |

| BIOS_ DIS1# | BIOS_ DIS0# | Chipset SPI CS1# Destination | Chipset SPI CS0# Destination | Carrier SPI_CS# | SPI Descriptor | BIOS Entry | Ref Line |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Module | Module | High | Module | SPI0/SPI1 | 0 |
| 1 | 0 | Module | Module | High | Module | Carrier FWH | 1 |
| 0 | 1 | Module | Carrier | SPI0 | Carrier | SPI0/SPI1 | 2 |
| 0 | 0 | Carrier | Module | SPI1 | Module | SPI1/SPI1 | 3 |

# 4.19 Watchdog Timer




## 4.19.1 Board Design

The Watchdog Timer (WDT) is implemented by Fintek F81801 Super IO.

| Register | Address |
|---|---|
| WDT Base Address | 0xA00 |

## 4.19.2 Psuedo Code

■ *Set WDT Time Unit (Second Unit)*

```
Step1: ByteData = ReadIOByte(0xA05)        //Read current setting
Step2: ByteData = ByteData & 0xF7          //Set time unit to "second"
Step3: WriteIOByte(0xA05, ByteData)        //Write back
```

■ *Set WDT Time Value*

```
Step1: WriteIOByte(0xA06, Time)            //Set watch dog time value
```

■ *Enable WDT*

```
Step1: ByteData = ReadIOByte(0xA05)        //Read current setting
Step2: ByteData = ByteData | 0x20          //Enable WDT
Step3: WriteIOByte(0xA05, ByteData)        //Write back
```

Chapter 5

# Driver Installation

# 5. Driver Installation

The drivers for the CE-ABT01 can be found on the driver DVD included with the system.

Install the following drivers in the order listed.

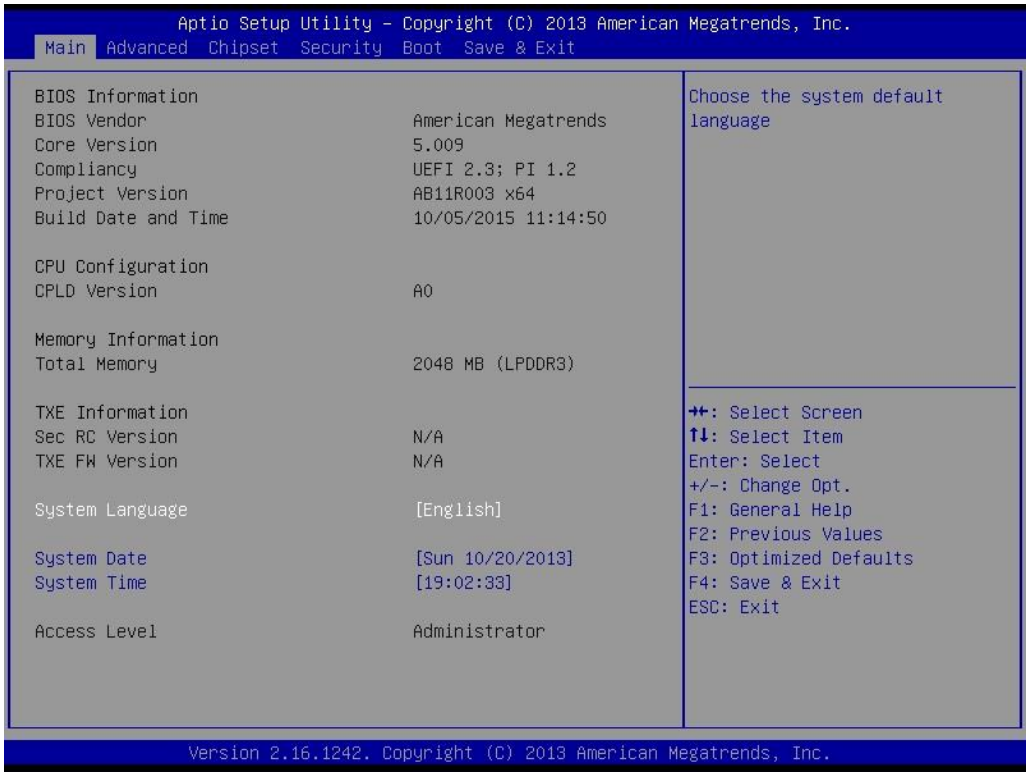
1. Chipset
2. Graphics
3. Audio
4. LAN
5. Intel Sideband Fabric Device (Intel MBI)
6. GPIO
7. Intel Trusted Execution Engine (Intel TXE)
8. $I^2C$
9. USB 3.0

Chapter 6

# System BIOS

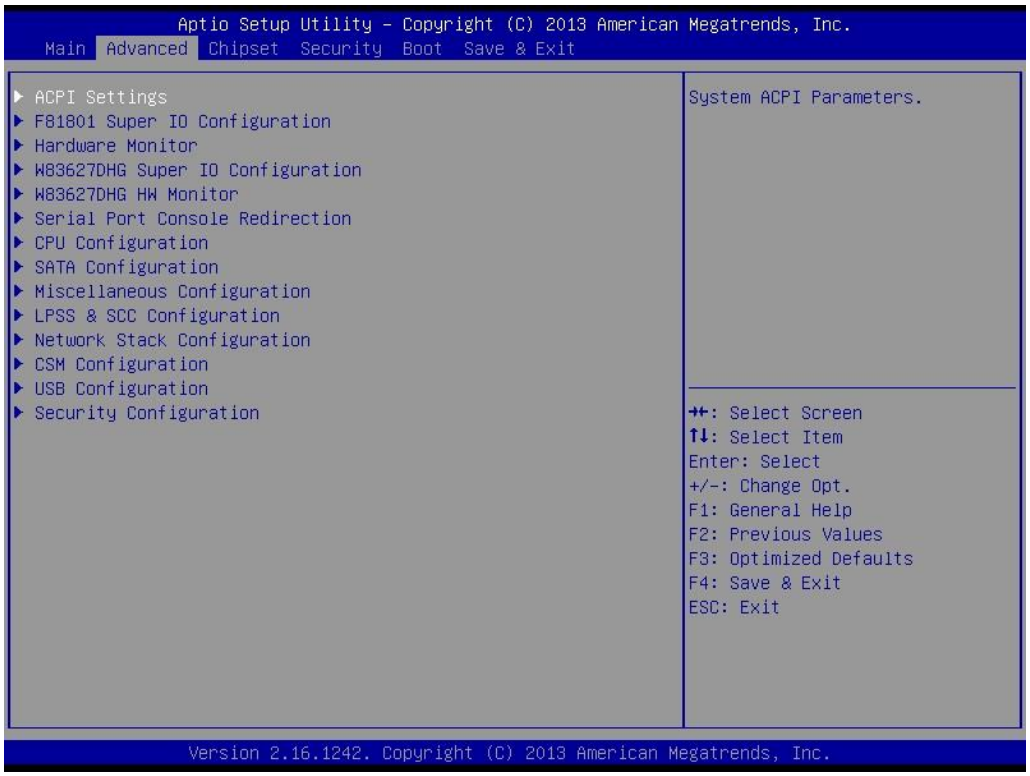
# 6. System BIOS

The system BIOS software is stored on EEPROM. The BIOS provides an interface to modify the configuration. When the battery is removed, all the parameters will be reset.
Turn on the computer and press <DEL> or <F2> to enter the setup screens.

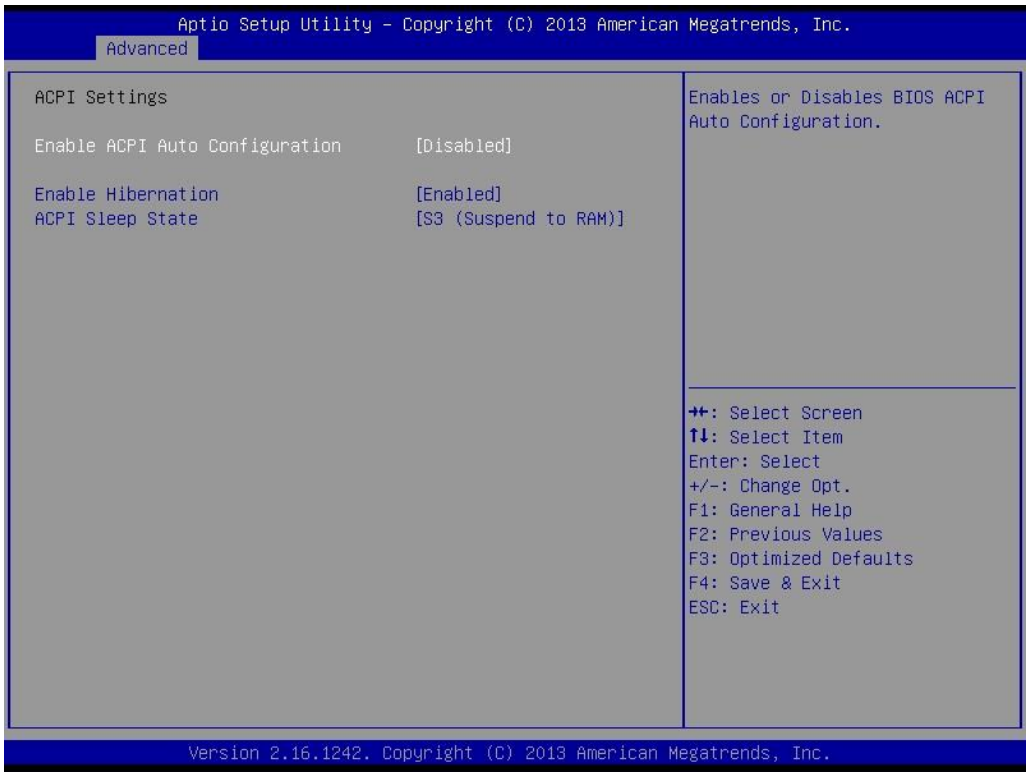



**System Date:** MM/DD/YYYY
**System Time:** HH:MM:SS
Use Tab to switch between Date and Time elements.

## 6.1 Advanced



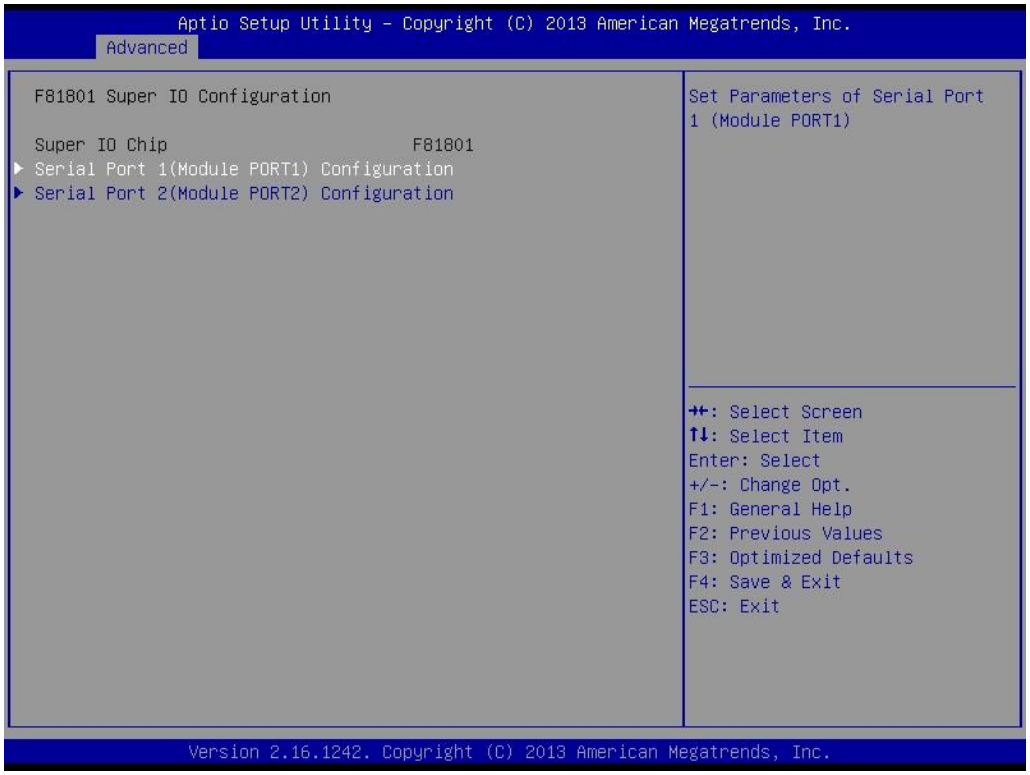
### 6.1.1 ACPI Settings




**Enable ACPI Auto Configuration:** Enables or disables BIOS ACPI Auto Configuration.
**Enable Hibernation:** Enable or Disable system ability to Hibernate.
**ACPI Sleep state:** Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed. Options: Suspend Disable, S3 (Suspend to RAM).

### 6.1.2 F81801 Super IO Configuration

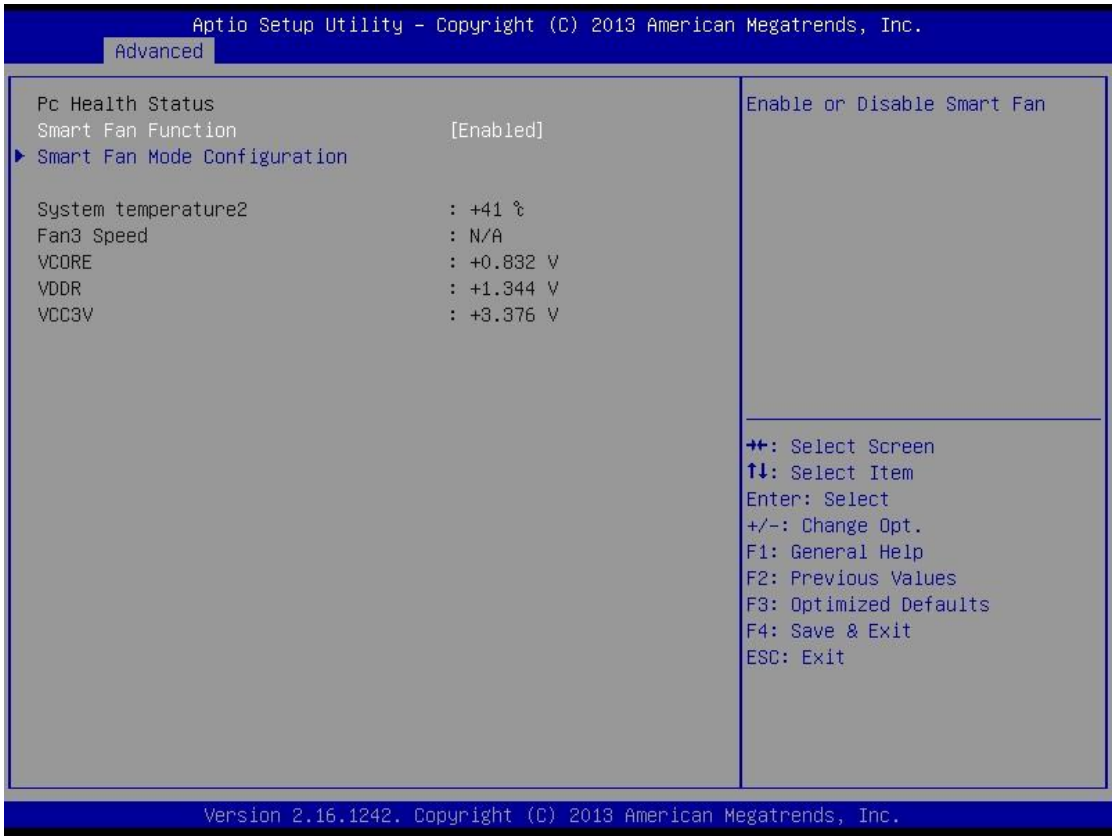
The F81801 Super IO is on the CE-ABT01 module. Enable/disable and configure the module serial ports.



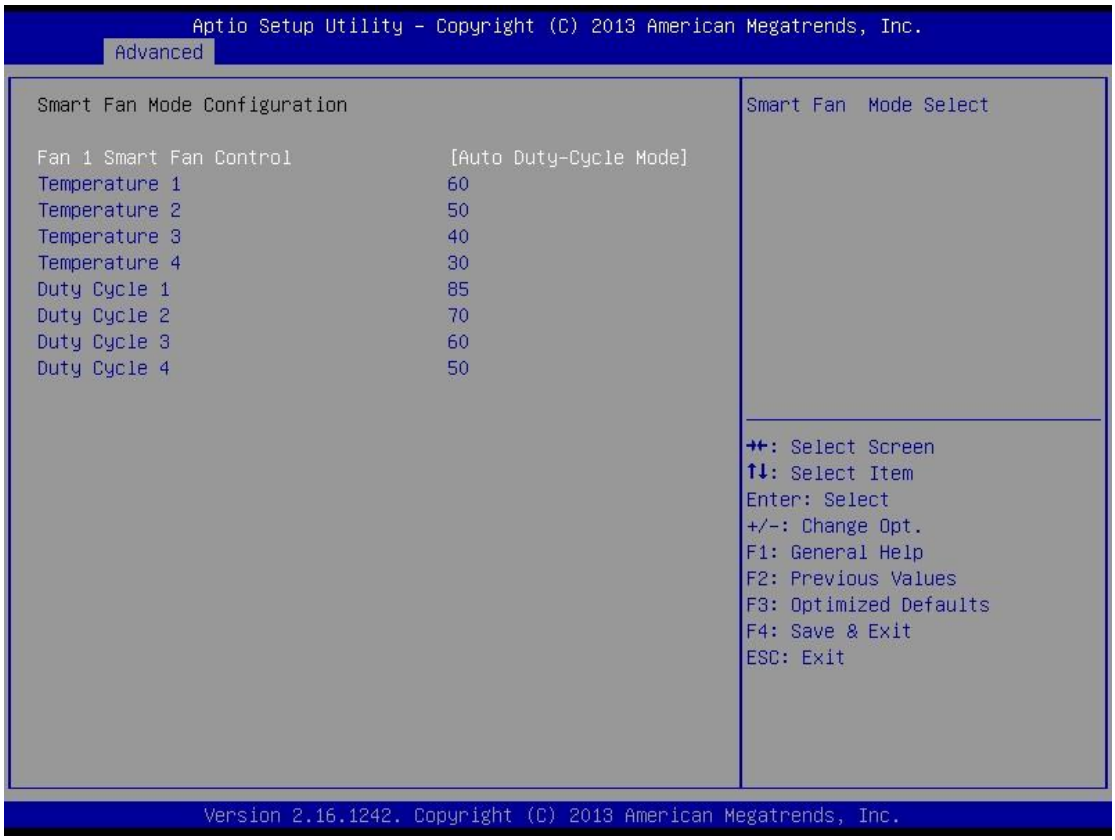
### 6.1.2.1 Serial Port 1/2 Configuration



## 6.1.3 Hardware Monitor

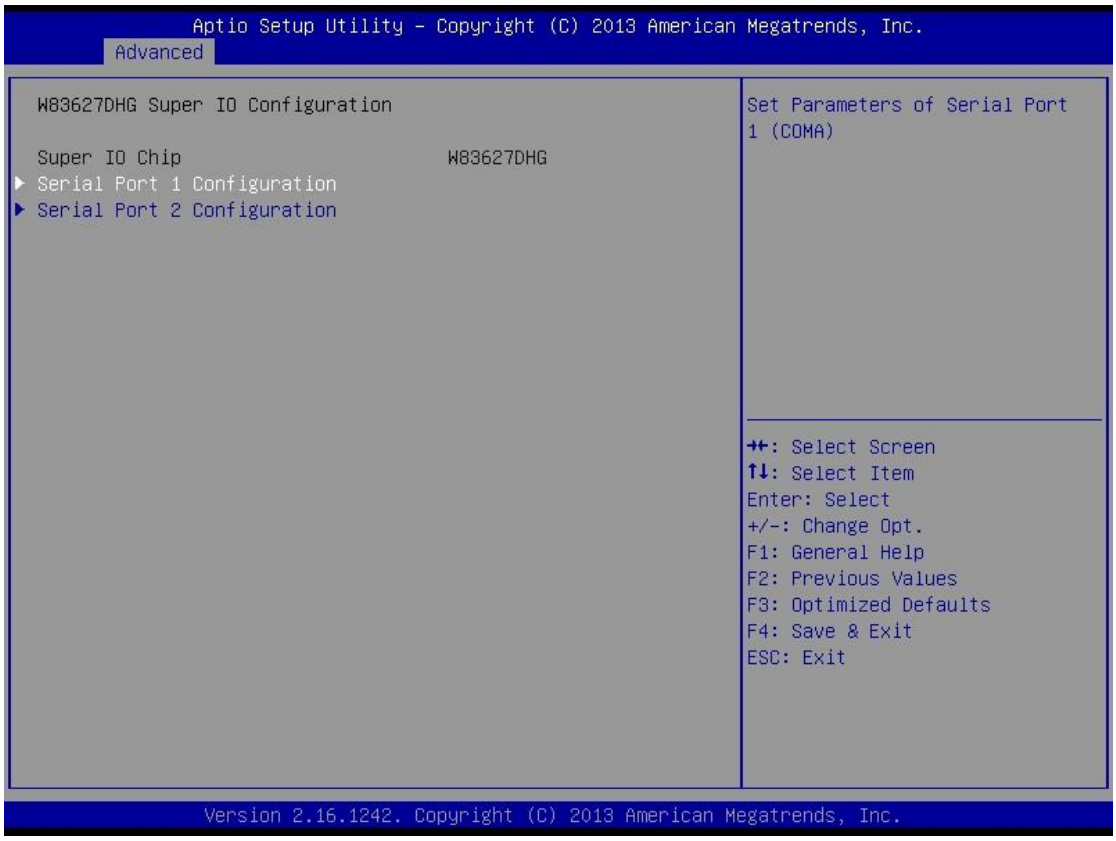


### 6.1.3.1 Smart Fan Mode Configuration




## 6.1.4 W83627DHG Super IO Configuration

The W83627DHG Super IO is on the CT-BTA01 carrier board. Enable/disable and configure the module serial ports.

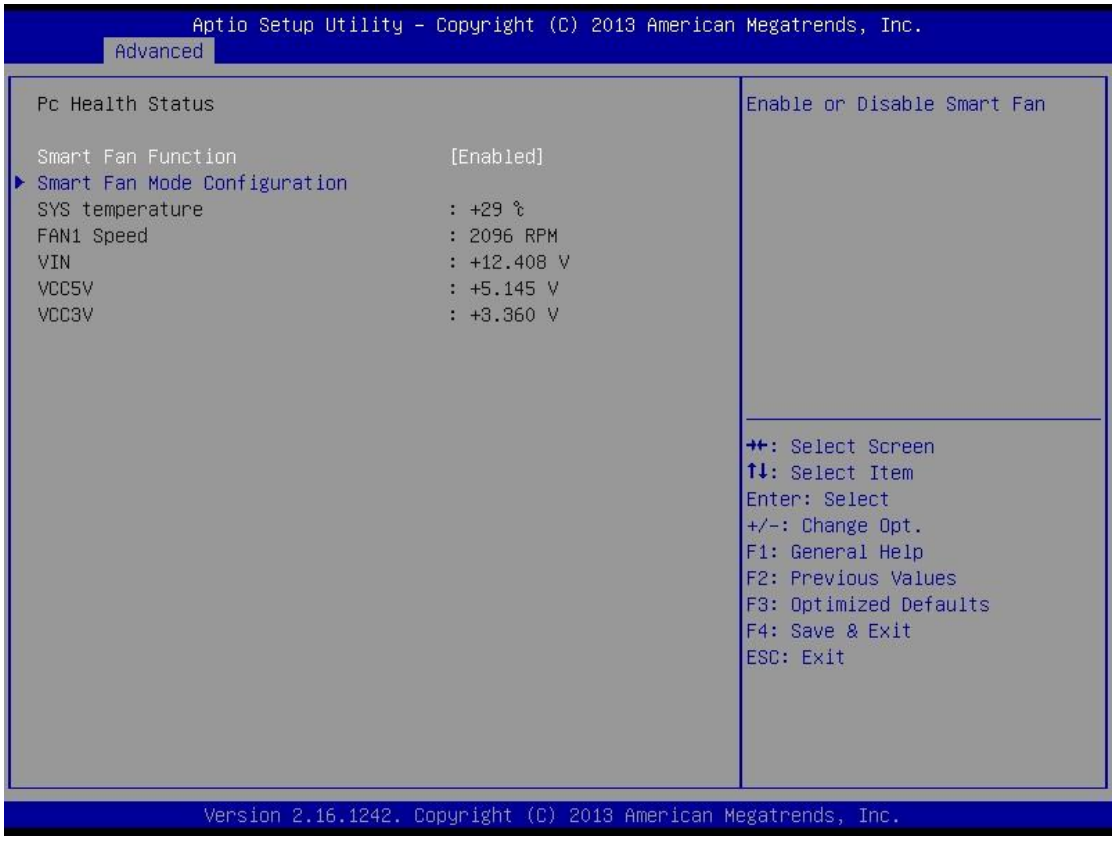


#### 6.1.4.1 Serial Port 1/2 Configuration



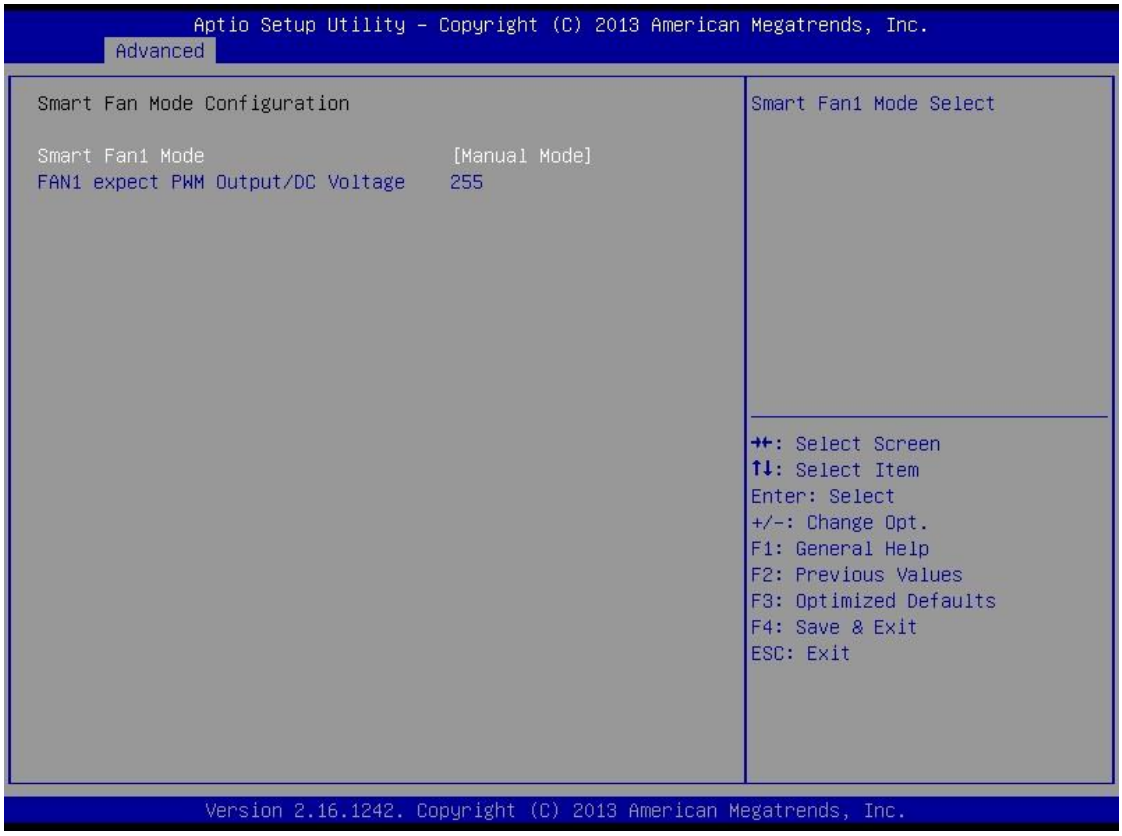
### 6.1.5 W83627DHG Hardware Monitor1

The W83627DHG Super IO is on the CT-BTA01 carrier board. Temperatures and voltages reported are from the carrier board.



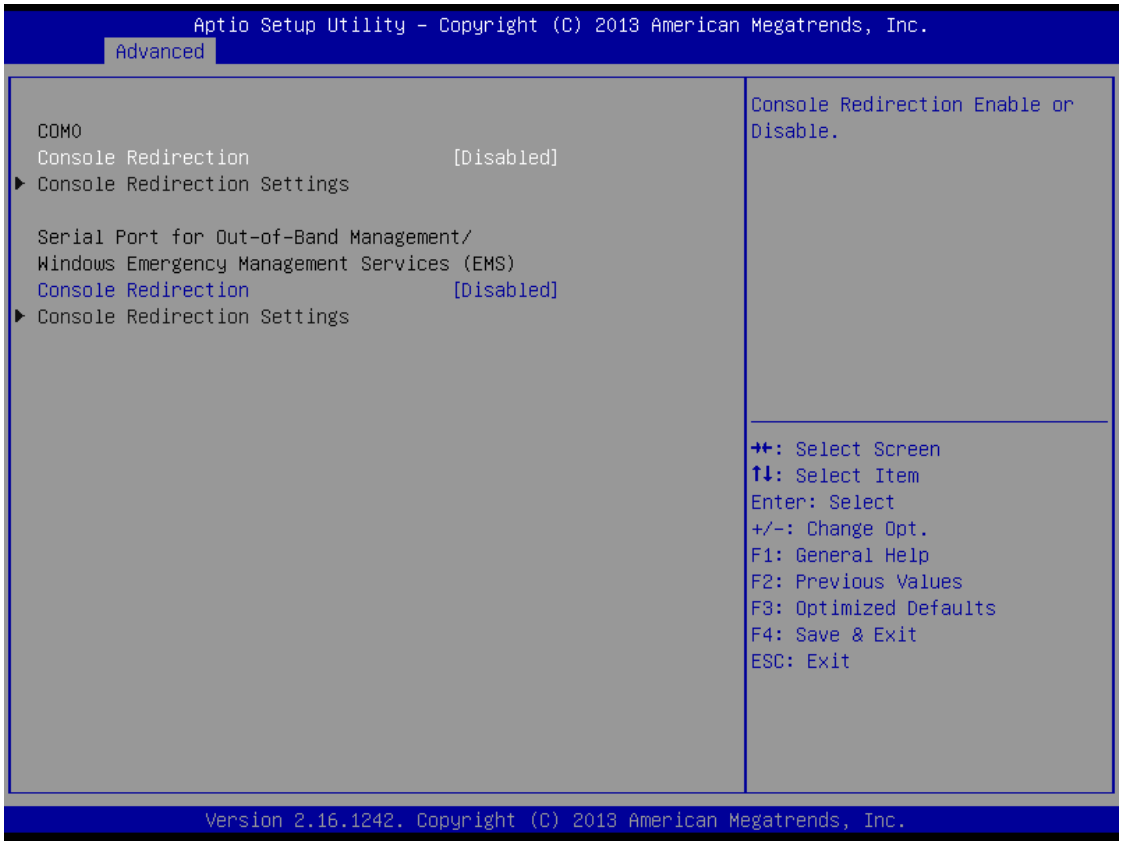
### 6.1.5.1 Smart Fan1 Mode Configuration

Smart Fan1 is controlled by the W83627DHG Super IO on the CT-BTA01 carrier board.




## 6.1.6 Serial Port Console Redirection

Serial port console redirection settings.



## 6.1.7 CPU Configuration

```
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Advanced

CPU Configuration                                   Socket specific CPU Information

▶ Socket 0 CPU Information

  CPU Speed                          2001 MHz
  64-bit                             Supported

  Intel Virtualization Technology    [Enabled]
  Power Technology                   [Energy Efficient]

                                                    →←: Select Screen
                                                    ↑↓: Select Item
                                                    Enter: Select
                                                    +/-: Change Opt.
                                                    F1: General Help
                                                    F2: Previous Values
                                                    F3: Optimized Defaults
                                                    F4: Save & Exit
                                                    ESC: Exit

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```

**Intel Virtualization Technology:** When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology
**Power Technology:** Configure the power management features.

### 6.1.7.1 CPU Information

```
Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
Advanced

Socket 0 CPU Information

Intel(R) Celeron(R) CPU J1900 @ 1.99GHz
CPU Signature                        30678
Microcode Patch                      815
Max CPU Speed                        1990 MHz
Min CPU Speed                        1334 MHz
Processor Cores                      4
Intel HT Technology                  Not Supported
Intel VT-x Technology                Supported

L1 Data Cache                        24 kB x 4
L1 Code Cache                        32 kB x 4
L2 Cache                             1024 kB x 2
L3 Cache                             Not Present

                                                    →←: Select Screen
                                                    ↑↓: Select Item
                                                    Enter: Select
                                                    +/-: Change Opt.
                                                    F1: General Help
                                                    F2: Previous Values
                                                    F3: Optimized Defaults
                                                    F4: Save & Exit
                                                    ESC: Exit

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```
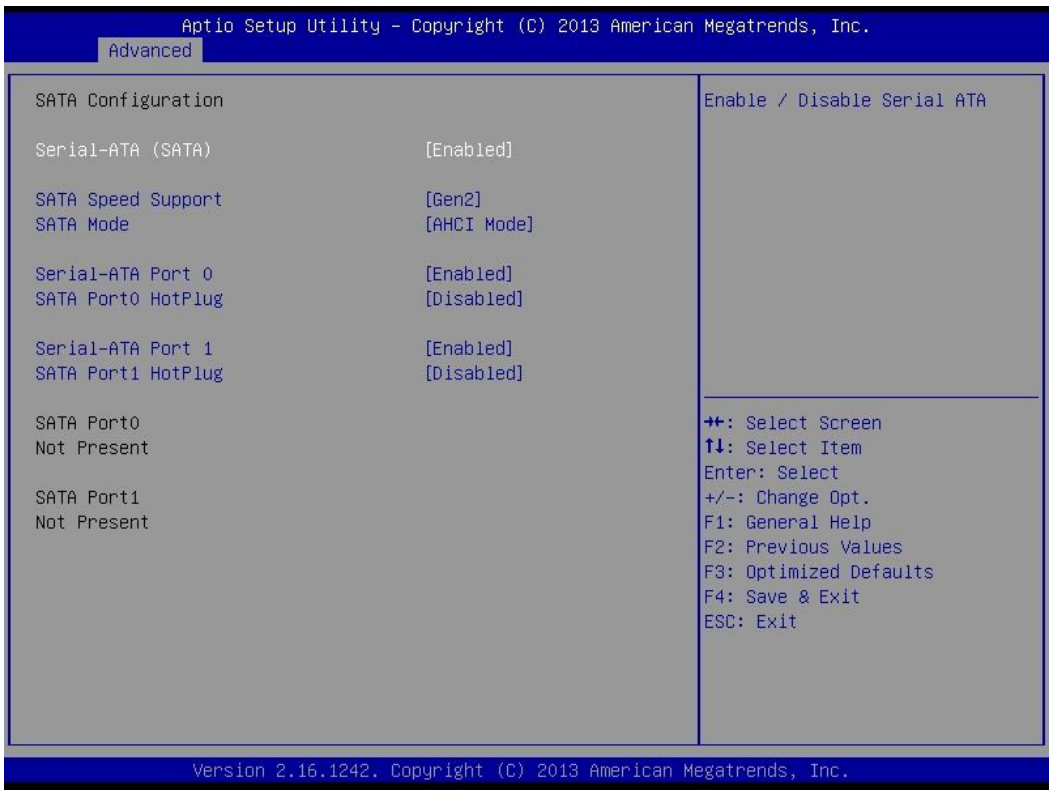
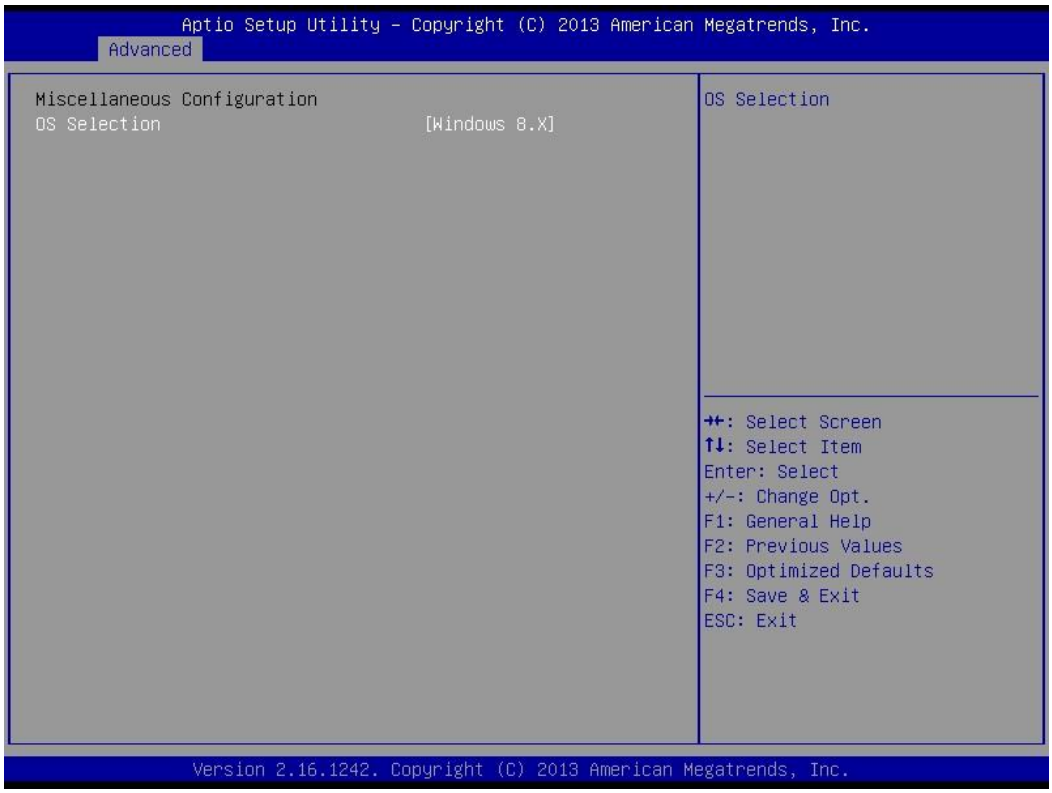

### 6.1.8 SATA Configuration

The BIOS automatically detects the presence of SATA device and the hardware installed in the SATA ports will be showed in the configuration. Each port can be enabled or disabled individually.




**SATA Speed Support:** Options: Gen 1, Gen 2.
**SATA Mode:** Select IDE or AHCI Mode
**SATA Port Hot Plug:** Enable/disable the port as Hot Pluggable.

### 6.1.9 Miscellaneous Configuration




OS Selection: Select the OS.

### 6.1.10 LPSS & SCC Configuration

```
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Advanced

SD/GPIO Select mode                [SD mode]
SCC Configuration
eMMC Secure Erase                  [Disabled]
SCC SD Card Support                [Enabled]
SDR25 Support for SDCard           [Disabled]
DDR50 Support for SDCard           [Enabled]
LPSS I2C #1 Support                [Disabled]

Select SD/GPIO mode in Carrier
Board

→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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```

**SCC eMMC Secure Erase:** Options: Disabled, Enabled.

### 6.1.11 Network Stack Configuration

```
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Advanced

Network Stack                      [Disabled]

Enable/Disable UEFI Network
Stack

→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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```
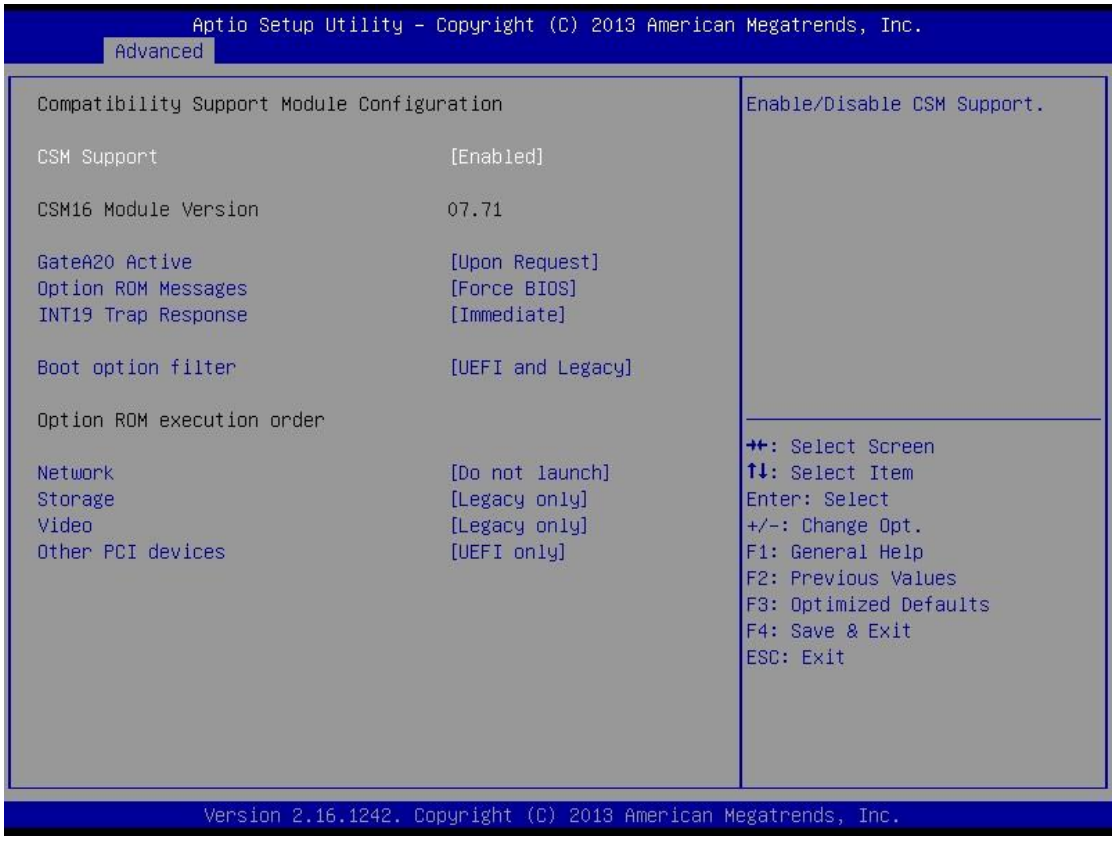

### 6.1.12 CSM Configuration




**GateA20 Active:**

[Upon Request] – GA20 can be disabled using BIOS services.

[Always] – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

**Option ROM Message:** Set display mode [Force BIOS] or [Keep Current] for Option ROM.

**INT19 Trap Response:** BIOS reaction on INT19 trapping by Option ROM: IMMEDIATE – execute the trap right away; POSTPONED – execute the traps during legacy boot.

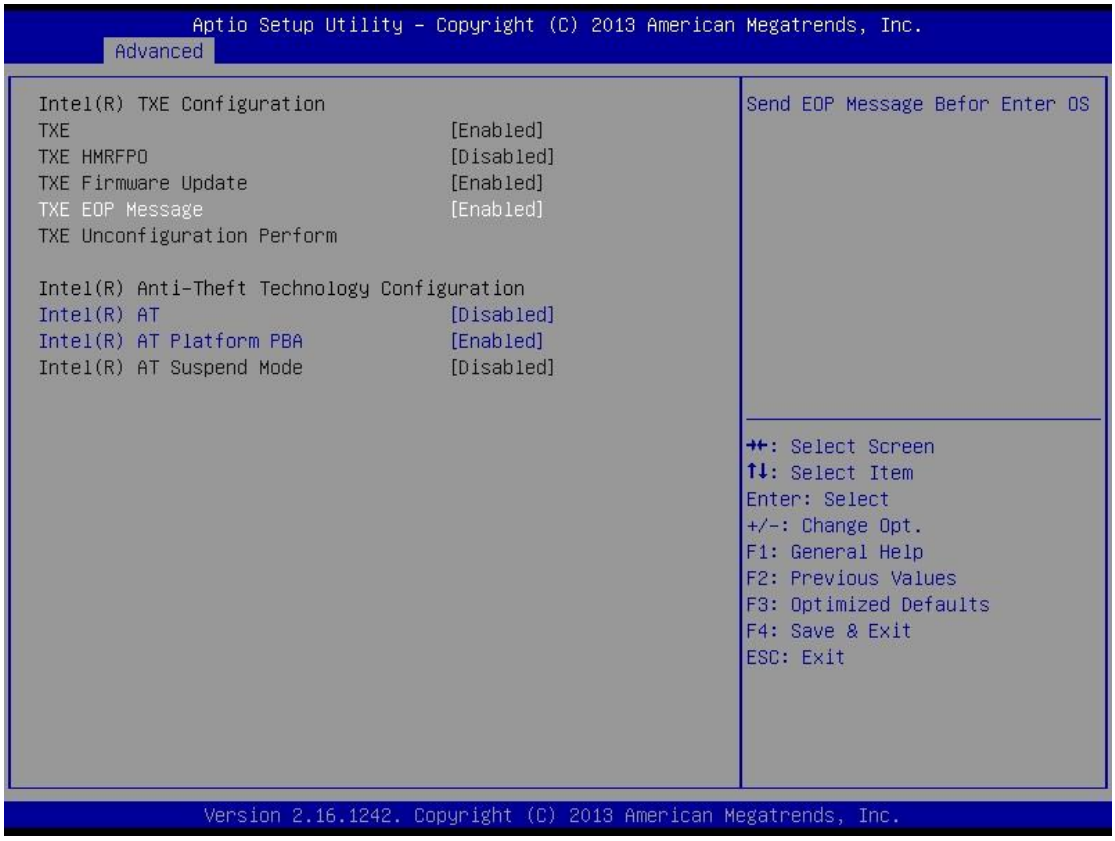
**Boot option filter:** This option controls what devices system can boot to [UEFI and Legacy], [Legacy only] or [UEFI only].

**Option ROM Execution Order:** Controls the execution Option ROM, [Do not launch], [UEFI only] or [Legacy only].

### 6.1.13 USB Configuration

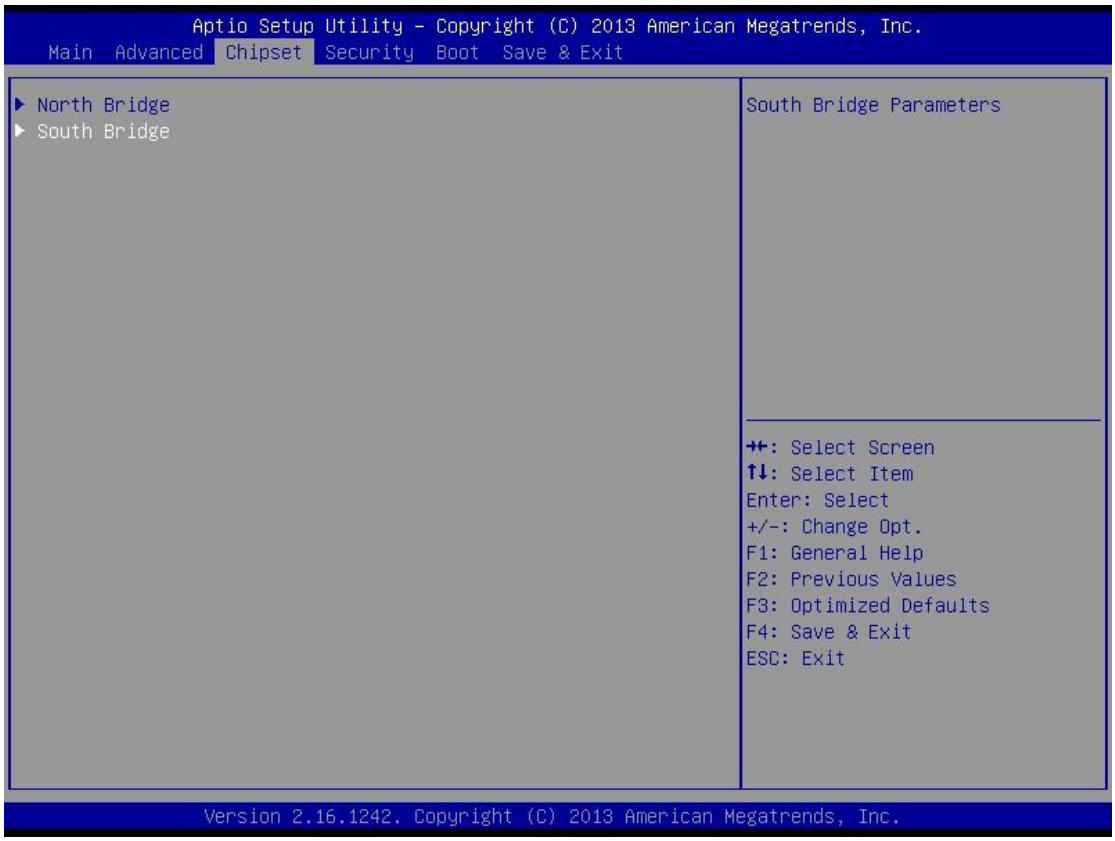

**Legacy USB Support:** Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications.
**XHCI Hand-off:** This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
**EHCI Hand-off:** This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.
**USB Mass Storage Driver Support:** Enable/Disable USB Mass Storage Driver Support.
**USB transfer time-out:** The time-out value for Control, Bulk, and Interrupt transfers.
**Device reset time-out:** USB mass storage device Start Unit command time-out.
**Device power-up delay:** Maximum time the device will take before it properly reports itself to the Host Controller. "Auto" uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

### 6.1.14 Security Configuration

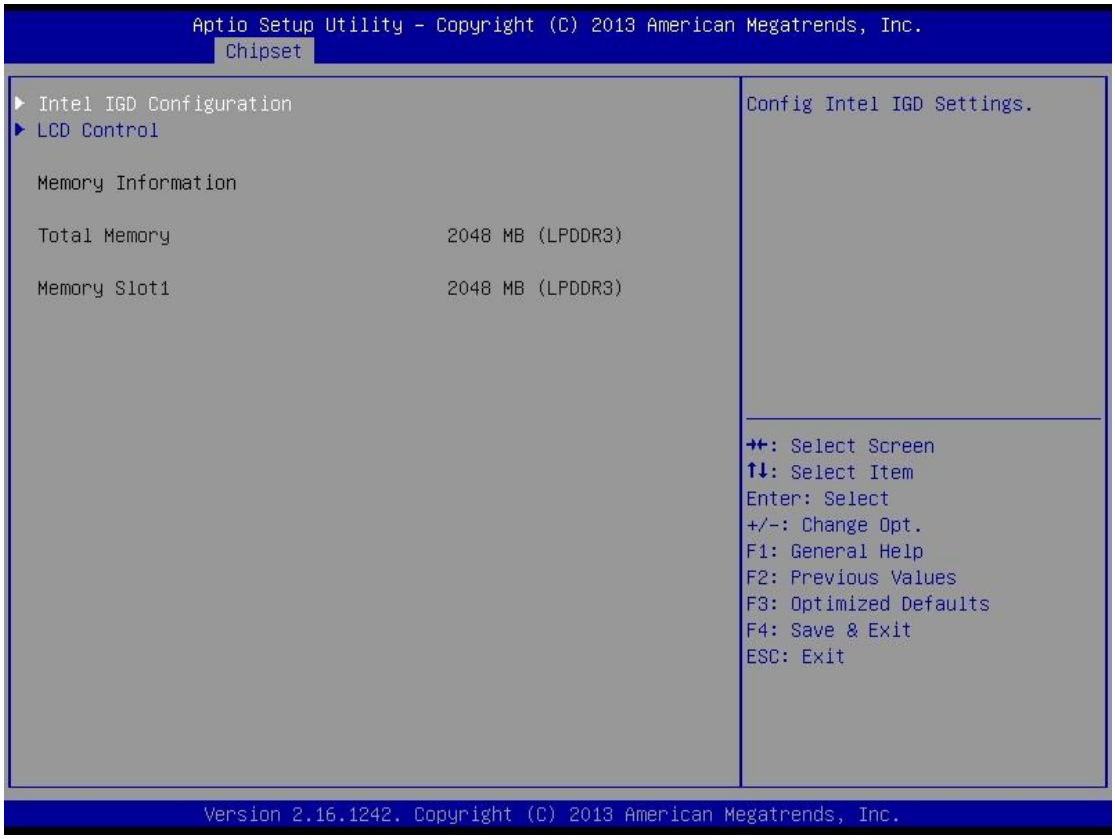



**TXE EOP Message:** Send EOP Message Before Enter OS.
**Intel® AT:** Enable/Disable BIOS AT Code from Running.
**Intel® AT Platform PBA:** Enable/Disable BIOS AT Code from Running.

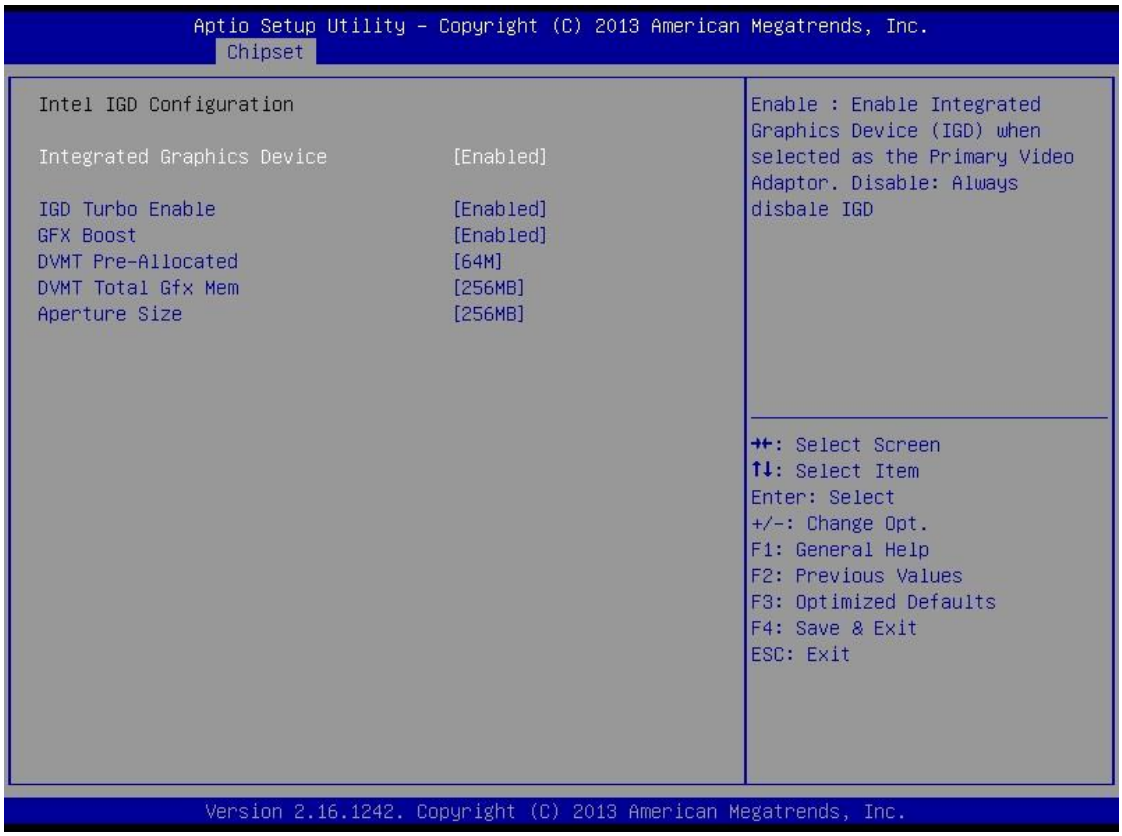
# 6.2 Chipset




## 6.2.1 Northbridge Configuration

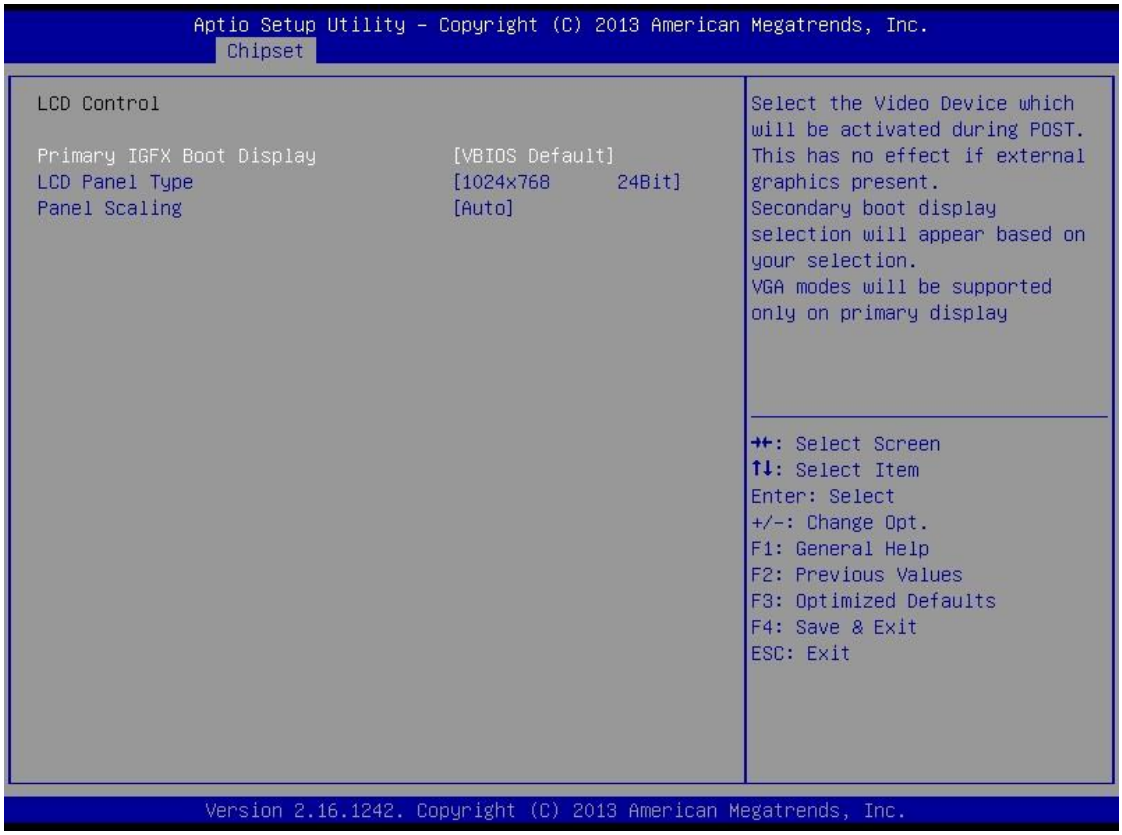


### 6.2.1.1 Intel IGD Configuration

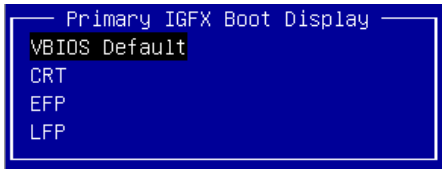



**Integrated Graphics Device:** Enable: Enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disable: Always disable IGD.
**IGD Turbo Enable:** Enable/Disable: IGD Turbo.
**GFX Boost:** Enable/Disable GFX Boost.
**DVMT Pre-Allocated:** Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
**DVMT Total Gfx Mem:** Select DVMT 5.0 Total Graphics Memory size used by the Internal Graphics Device.
**Aperture Size:** Select the Aperture Size.

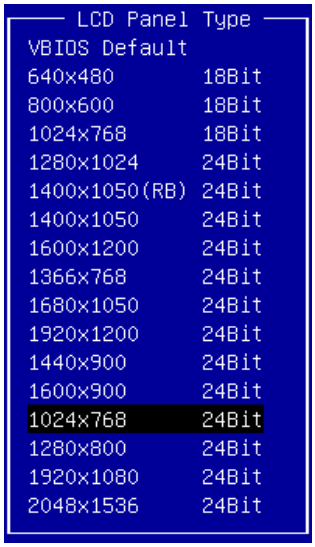
### 6.2.1.2 LCD Control




**Primary IGFX Boot Display:** Default setting is "VBIOS Default". "CRT" is VGA, "EFP" is DisplayPort, "LFP" is LVDS.




**LCD Panel Type: Default setting is "1024x768 24-bit".**



## 6.2.2 Southbridge Configuration

```
Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
                    Chipset

▶ USB Configuration                                  USB Configuration Settings
▶ PCI Express Configuration

  High Precision Timer                 [Enabled]
  Restore AC Power Loss                [Last State]
  Onboard LAN                          [Enabled]

                                                    →←: Select Screen
                                                    ↑↓: Select Item
                                                    Enter: Select
                                                    +/-: Change Opt.
                                                    F1: General Help
                                                    F2: Previous Values
                                                    F3: Optimized Defaults
                                                    F4: Save & Exit
                                                    ESC: Exit

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```

**High Precision Timer:** Enable or Disable the High Precision Event Timer.
**Restore AC Power Loss:** Select AC power state when power is re-applied after a power failure.

### 6.2.2.1 USB Configuration

```
Aptio Setup Utility - Copyright (C) 2013 American Megatrends, Inc.
                    Chipset

  USB Configuration                                 Enable/Disable USB OTG Support
  USB OTG Support                      [Disabled]
  USB VBUS                             [Off]

  XHCI Mode                            [Enabled]

  USB RMH Mode                         [Enabled]
  USB EHCI debug                       [Disabled]
  USB Per Port Control                 [Enabled]
  USB 3.0 Port                         [Enabled]
  USB Port 1 (to USB Hub)              [Enabled]
  USB Port 2                           [Enabled]
  USB Port 3                           [Enabled]
                                                    →←: Select Screen
                                                    ↑↓: Select Item
                                                    Enter: Select
                                                    +/-: Change Opt.
                                                    F1: General Help
                                                    F2: Previous Values
                                                    F3: Optimized Defaults
                                                    F4: Save & Exit
                                                    ESC: Exit

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```
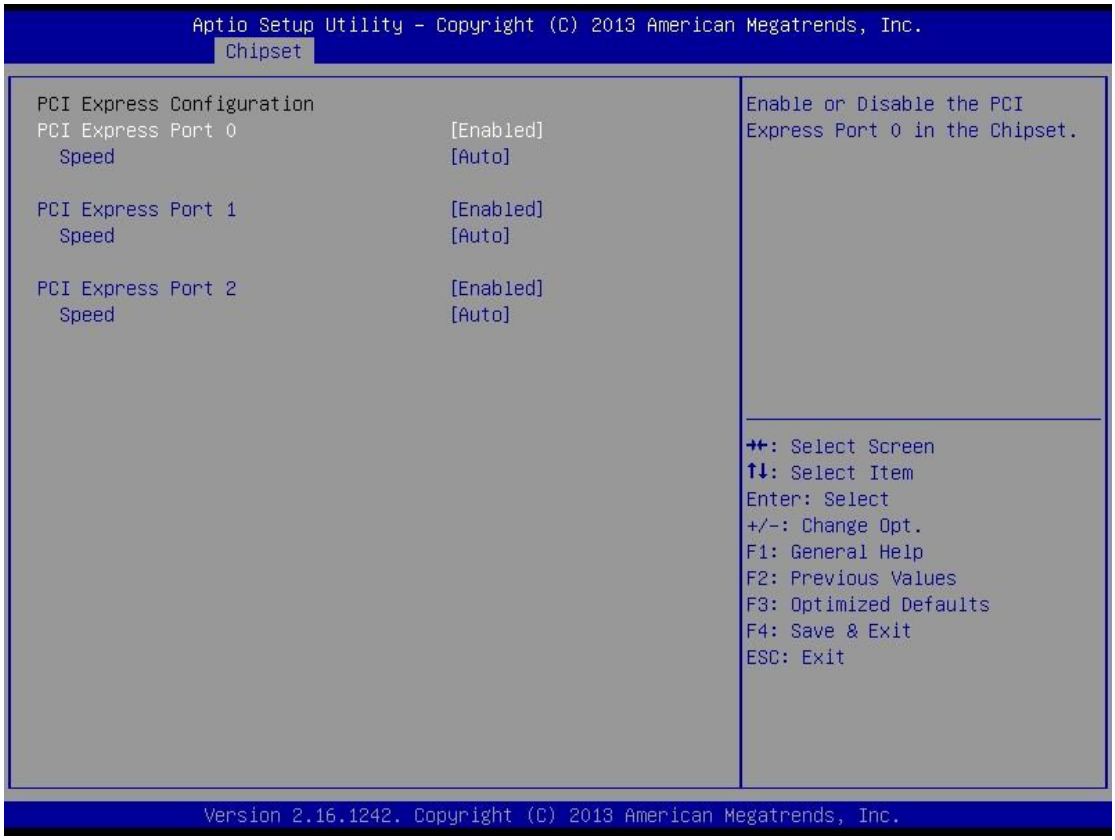
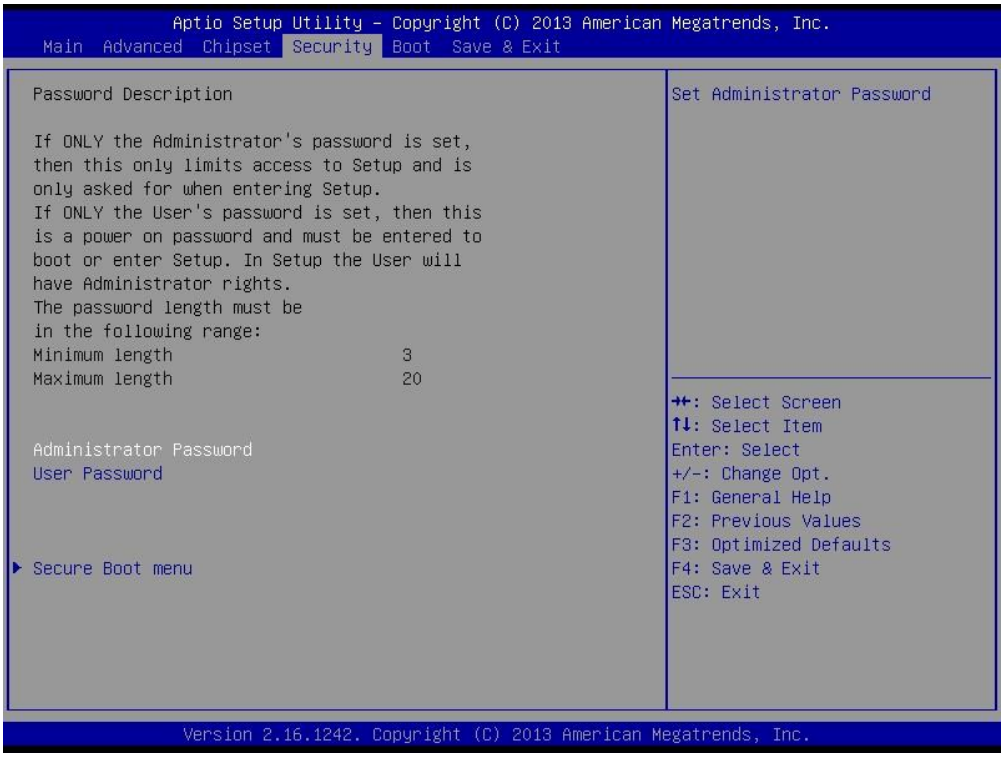

### 6.2.2.2 PCI Express Configuration

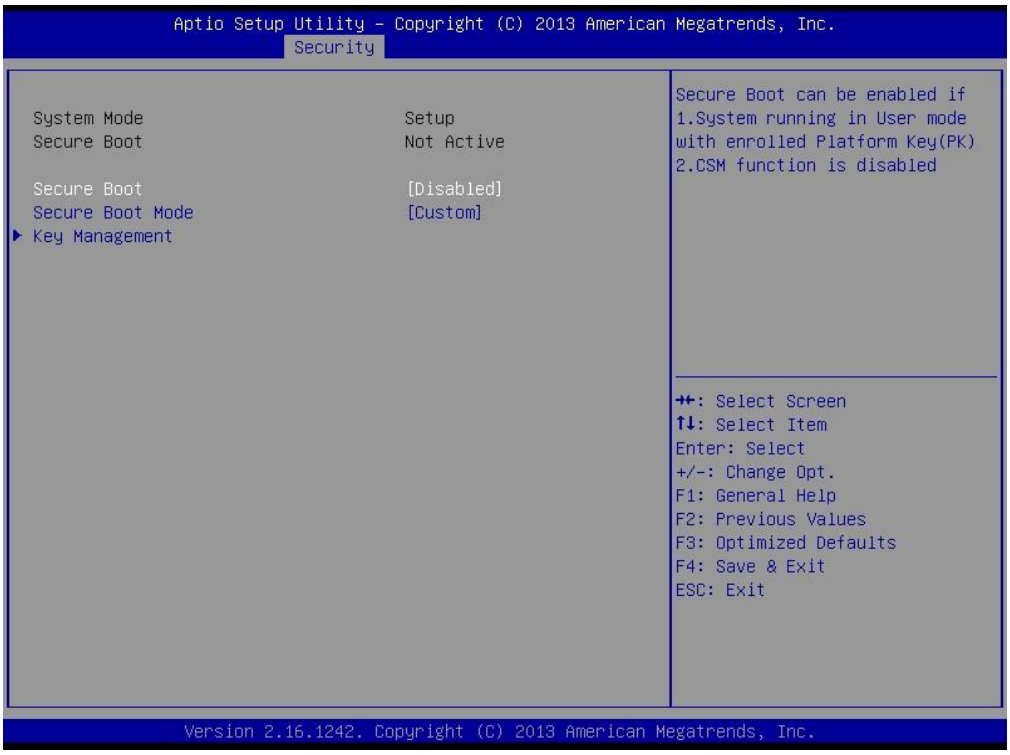


## 6.3 Security

Administrator's and User's passwords could be set.
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup, the user will have administrator rights. The minimum length of the password is 3 and the maximum length is 20.

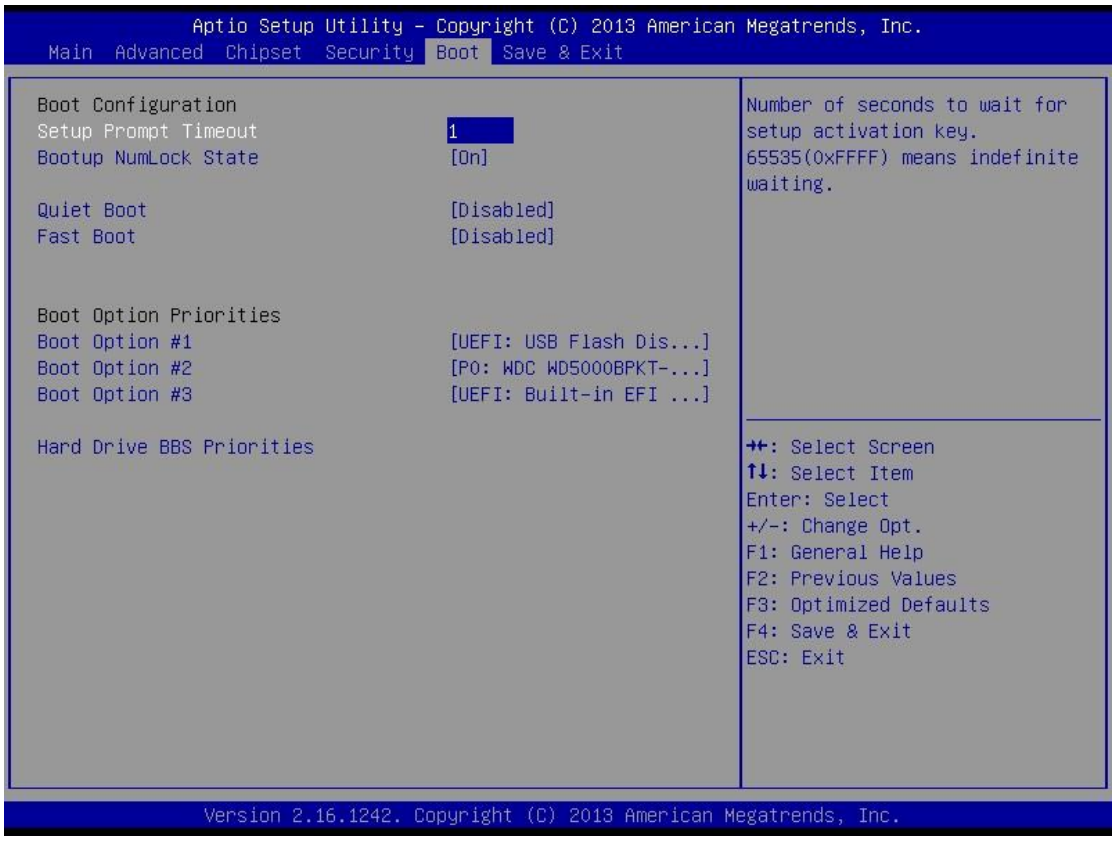



### 6.3.1 Secure Boot Menu




**Secure Boot:** Secure Boot can be enabled if the System running in User mode with enrolled Platform Key (PK) and CSM function is disabled.
**Secure Boot Mode:** Secure Boot mode selector. 'Custom' Mode enables users to change Image Execution policy and manage Secure Boot Keys.

## 6.4 Boot




**Setup Prompt Timeout:** Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
**Bootup NumLock State:** Select [Enable] or [Disable] for the keyboard NumLock state.
**Quiet Boot:** Enables or disables Quiet Boot option.
**Fast Boot:** Enables or disables Fast Boot option.
**Boot Option Priorities:** Set the system boot order.
**Hard Drive BBS Priorities:** Set the order of the legacy devices in this group.

## 6.5 Save and Exit