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DSL Ltd. | 4 Aylesford Court, Works Road, Letchworth Garden City, Hertfordshire, SG6 1LP

TS16GSSD630 **TS96GSSD630**
TS32GSSD630 **TS128GSSD630**
TS64GSSD630 **TS256GSSD630**

2.5'' SATA II Solid State Disk

Description

Transcend's 2.5'' SATA II Solid State Disk comes in two different thicknesses (7mm or 9.5mm in height and both fit the standard dimensions of 2.5'' SATA Hard Disk Drives), huge capacity, high speed, and low power consumption, it is the perfect storage device for PCs, Laptops, gaming systems, and handheld devices.

- Fully compatible with devices and OS that support the SATA II 3.0Gb/s standard
- Non-volatile Flash Memory for outstanding data retention
- Support Trim and NCQ command

Features

- ROHS compliant
- Advanced Global Wear-Leveling and Block management for reliability
- Built-in ECC (Error Correction Code) functionality
- With DRAM Cache
- Advanced Garbage Collection
- Advanced Power Shield
- Support Security Command
- Support Enhanced S.M.A.R.T. function
- Hardware Purge and Write Protect
- Optional, support Transcend's SSD Scope Pro

General Dimensions

Ultra-Slim Model

Side	Millimeters	Inches
A	99.80 ± 0.25	3.929 ± 0.010
B	69.80 ± 0.25	2.748 ± 0.010
C	7.00 - 0.30	0.276 - 0.012

Standard Model

Side	Millimeters	Inches
A	100.30 ± 0.25	3.949 ± 0.010
B	69.85 ± 0.25	2.750 ± 0.010
C	9.50 ± 0.15	0.374 ± 0.006

Specifications

Physical Specification		Ultra-Slim Model	Standard Model
Form Factor		2.5-inch SSD	
Storage Capacities		16 GB to 256 GB	
Dimensions (mm)	**Length**	99.80 ± 0.25	100.30 ± 0.25
	Width	69.80 ± 0.25	69.85 ± 0.25
	Height	7.00 - 0.30	9.50 ± 0.15
Input Voltage		5V ± 5%	
Weight (g)		48 ± 2	64 ± 2
Connector		SATA 22 pins connector	

Environmental Specifications		
Operating Temperature		0 ℃ to 70 ℃
Storage Temperature		- 40 ℃ to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Performance

Model P/N	Sequential Read*	Sequential Write*	Random Read (4KB QD32)*	Random Write (4KB QD32)*	IOPS Random Read (4KB QD32)**	IOPS Random Write (4KB QD32)**
TS16GSSD630	120	20	65	15	13700	2100
TS32GSSD630	240	40	70	40	14400	3600
TS64GSSD630	260	85	70	65	14600	4100
TS96GSSD630	225	120	70	70	14200	4100
TS128GSSD630	255	150	70	70	14800	4600
TS256GSSD630	260	225	60	15	12600	2700

Note: Maximum transfer speed recorded
* 25 ℃, test on ASUS P8H77-M Pro + Intel Core i5, 2GB, Windows® 7 with AHCI mode, benchmark utility Crystal DiskMark (version 3.0), copied file 1000MB, unit MB/s
** Random read/write performance based on IOmeter2006 with 4K file size and queue depth of 32 at full size LBA address, unit IOPs
*** The recorded performance is obtained while the SSD is not operating as an OS disk

Actual Capacity				
Model P/N	**LBA**	**Cylinder**	**Head**	**Sector**
TS16GSSD630	31,277,232	16,383	16	63
TS32GSSD630	62,533,296	16,383	16	63
TS64GSSD630	125,045,424	16,383	16	63
TS96GSSD630	187,557,553	16,383	16	63
TS128GSSD630	250,069,680	16,383	16	63
TS256GSSD630	500,118,192	16,383	16	63

Power Consumption		
Input Voltage		5V ± 5%
Model P/N / Power Consumption		**Typical (mA)**
TS16GSSD630	**Read**	121
	Write	207
	Idle	153
TS32GSSD630	**Read**	160
	Write	237
	Idle	154
TS64GSSD630	**Read**	272
	Write	278
	Idle	165
TS96GSSD630	**Read**	301
	Write	422
	Idle	152
TS128GSSD630	**Read**	305
	Write	452
	Idle	150
TS256GSSD630	**Read**	332
	Write	569
	Idle	161

*Tested reads/writes with IOmeter running sequential and idle mode

Reliability		
Data Reliability	Supports BCH ECC 40 bit per 1024 byte	
MTBF	1,000,000 hours	
Endurance (TeraBytes Written)*	TS16GSSD630	17.0 (TB)
	TS32GSSD630	35.0 (TB)
	TS64GSSD630	76.0 (TB)
	TS96GSSD630	110.0 (TB)
	TS128GSSD630	175.0 (TB)
	TS256GSSD630	275.0 (TB)
Data Retention*	10 years when SSD is fresh out of the box 1 year when full TBW rating is reached	

*Note: Based on JEDEC JESD218A & 219A standard, Client Application Class with the following scenario:
Active use: 40°C, 8hrs/day; Retention use: 30°C

Vibration	
Operating	5.0G, 5 - 800Hz
Non-Operating	20.0G, 5 - 800Hz

Reference to IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

Reference to IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500G, 0.5ms, 3 times/dir., total 18 times.

Regulations	
Compliance	CE, FCC and BSMI

Features

- **Global Wear Leveling – Advanced algorithm to enhance the Wear-Leveling Efficiency**

  There are 3 main processes in global wear leveling approaches:

  (1) Record the block erase count and save in the wear-leveling table.

  (2) Find the static-block and save it in wear-leveling pointer.

  (3) Check the erase count when the block popped from spare pool. If the block erase count is larger than WEARCNT, then swap the static-block and over-count-block. After actual test, global wear leveling successfully even the erase count of every block; hence, it may extend the life expectancy of the SSD.

- **ECC Algorithm**

  The controller uses BCH40 ECC algorithm per 1024 bytes depending on the structure of the flash. BCH40 may correct up to 40 random error bits within 1024 data bytes. With the help of BCH40 ECC, the endurance of Transcend SSD is greatly improved.

- **Bad Block Management**

  When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as bad block. This will prevent the usage of bad blocks which may result in data loss in the future.

- **Advanced Garbage Collection**

  Transcend SSD has perfect garbage collection mechanism to improve the performance of SSD. Advanced Garbage collection can efficiently manage data memory which allows the SSD to always maintain a stable performance. With Transcend's advanced flash management, the drive will be able to maintain high transfer speed even after long period of usage.

- **Enhanced S.M.A.R.T. function**

  Transcend SSD supports S.M.A.R.T. command (Self-Monitoring, Analysis, and Reporting Technology) that allows the user to read the health information of the SSD. Transcend also defines some innovated S.M.A.R.T. features which allows the user to evaluate the status of the SSD in a much more efficient way.

- **Advanced Power Shield**

  The controller uses intelligent internal power shield circuit to prevent SSD from damage when sudden power off or during power failure. The internal power detection mechanism of the SSD can monitor the power provided by the host. When sudden power loss occurs, the SSD will execute advanced power shield mechanism to protect data in the SSD.

- **Hardware Purge and Write Protect**

  The SSD has built in hardware trigger for quick data erase and write protect of user data area. These features may be enabled by simply connecting a switch to the designated pins.

- **StaticDataRefresh Technology**

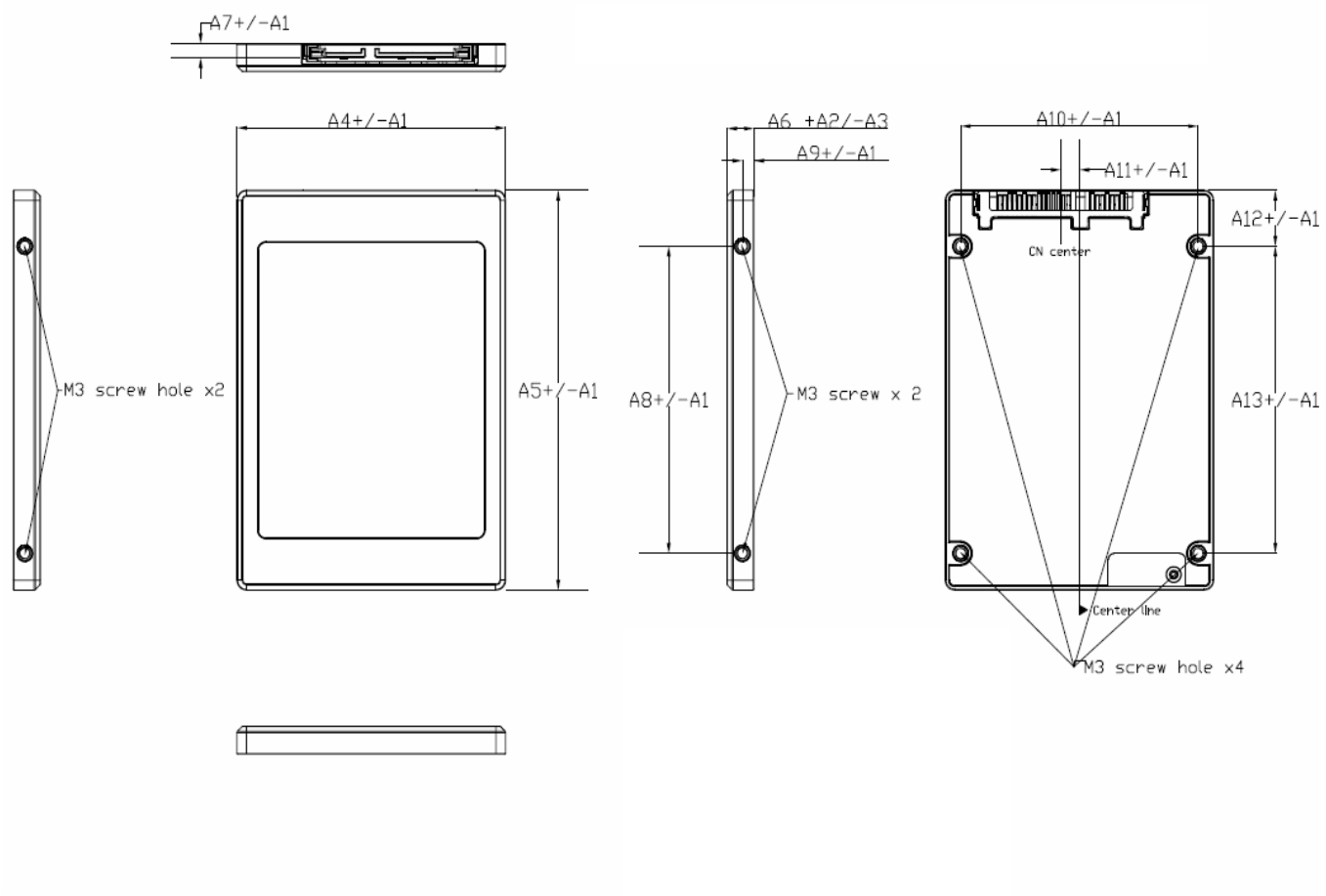
  Normally, ECC engine corrections are taken place without affecting the host normal operations. As time passes by, the number of error bits accumulated in the read transaction exceeds the correcting capability of the ECC engine, resulting in corrupted data being sent to the host. To prevent this, the controller monitors the error bit levels at each read operation; when it reaches the preset threshold value, the controller automatically performs data refresh to "restore" the correct charge levels in the cell. This implementation practically restores the data to its original, error-free state, and hence, lengthening the life of the data.

- **EarlyRetirement Technology**

  The StaticDataRefresh feature functions well when the cells in a block are still healthy. As the block ages over time, it cannot reliably store charge anymore and EarlyRetirement enters the scene. EarlyRetirement works by moving the static data to another block (a healthy block) before the previously used block becomes completely incapable of holding charges for data. When the charge loss error level exceeds another threshold value (higher from that for StaticDataRefresh), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevent it from further usage and make the block enters the state of "EarlyRetirement." Note that, through this process, the incorrect data are detected and effectively corrected by the ECC engine, thus the data in the new block is stored error-free.

Physical Dimensions (Ultra-Slim Model)

Below figure illustrates the Ultra-Slim Model of Transcend 2.5" SATA II Solid State Disk. All dimensions are in mm.

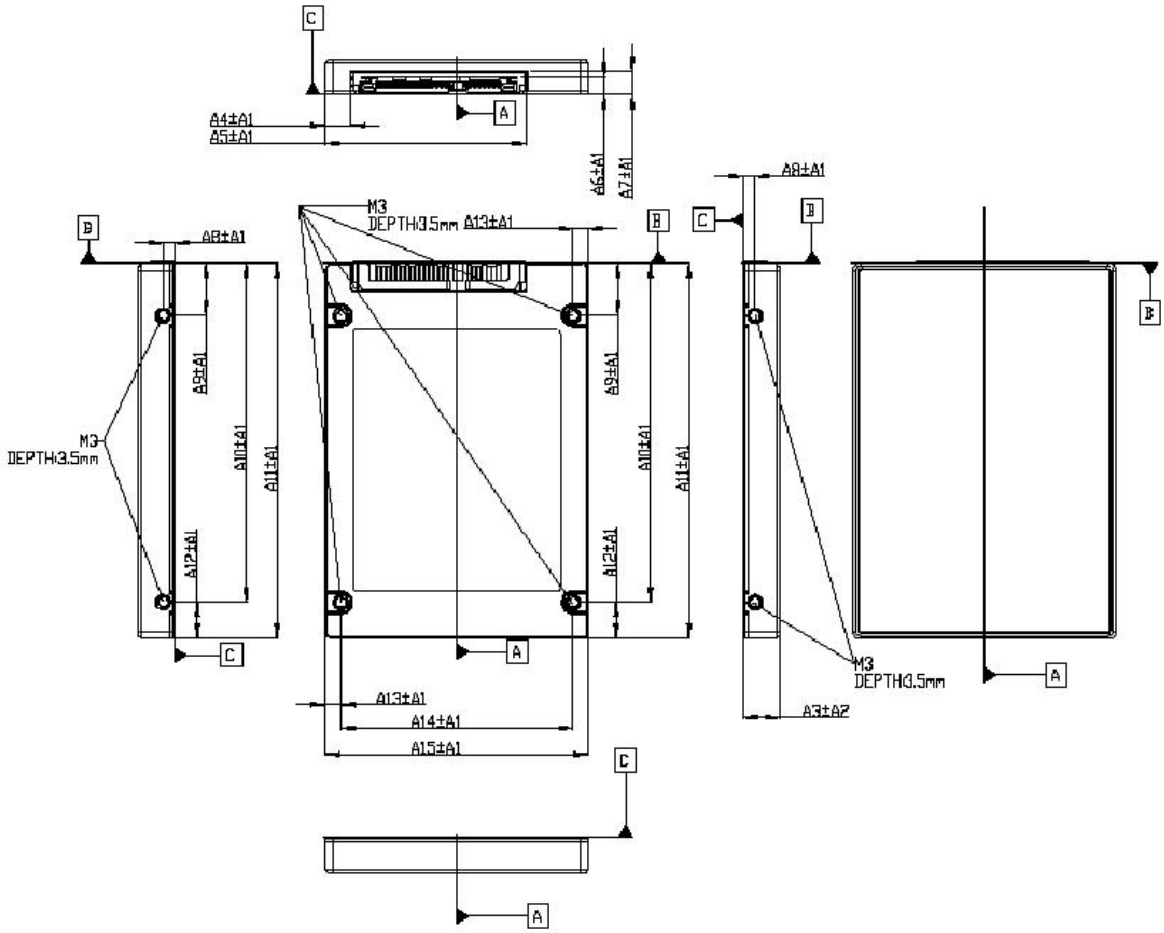


Item	Millimeter	Item	Millimeter
A1	0.25	A11	4.80
A2	0.00	A12	14.00
A3	0.30	A13	76.60
A4	69.80		
A5	99.80		
A6	7.00		
A7	3.5		
A8	76.60		
A9	3.00		
A10	61.72		

*Note: Tighten mounting screws with no more than 3.0 kgf-cm (0.22ft-lbs) of torque.

Physical Dimensions (Standard Model)

Below figure illustrates the 9.5mm Model of Transcend 2.5" SATA II Solid State Disk. All dimensions are in mm.



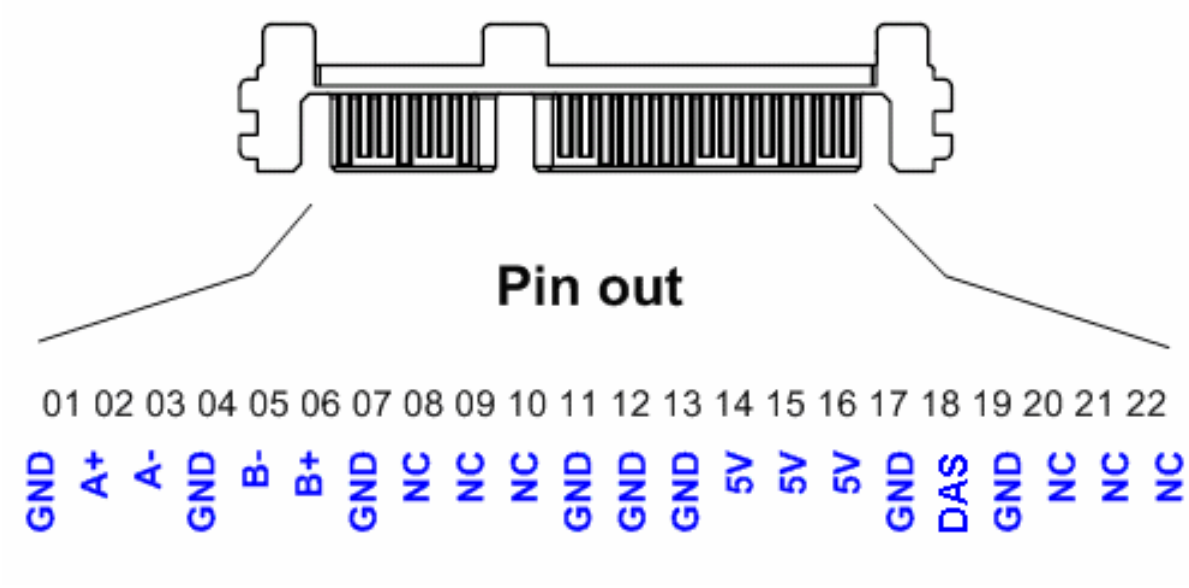
Dimension	Millimeter	Dimension	Millimeter
A1	0.25	A9	14.00
A2	0.15	A10	90.60
A3	9.50	A11	100.3
A4	6.75	A12	9.70
A5	53.52	A13	4.06
A6	4.93	A14	61.72
A7	6.34	A15	69.85
A8	3.00		

*Note: Tighten mounting screws with no more than 3.0 kgf-cm (0.22ft-lbs) of torque.

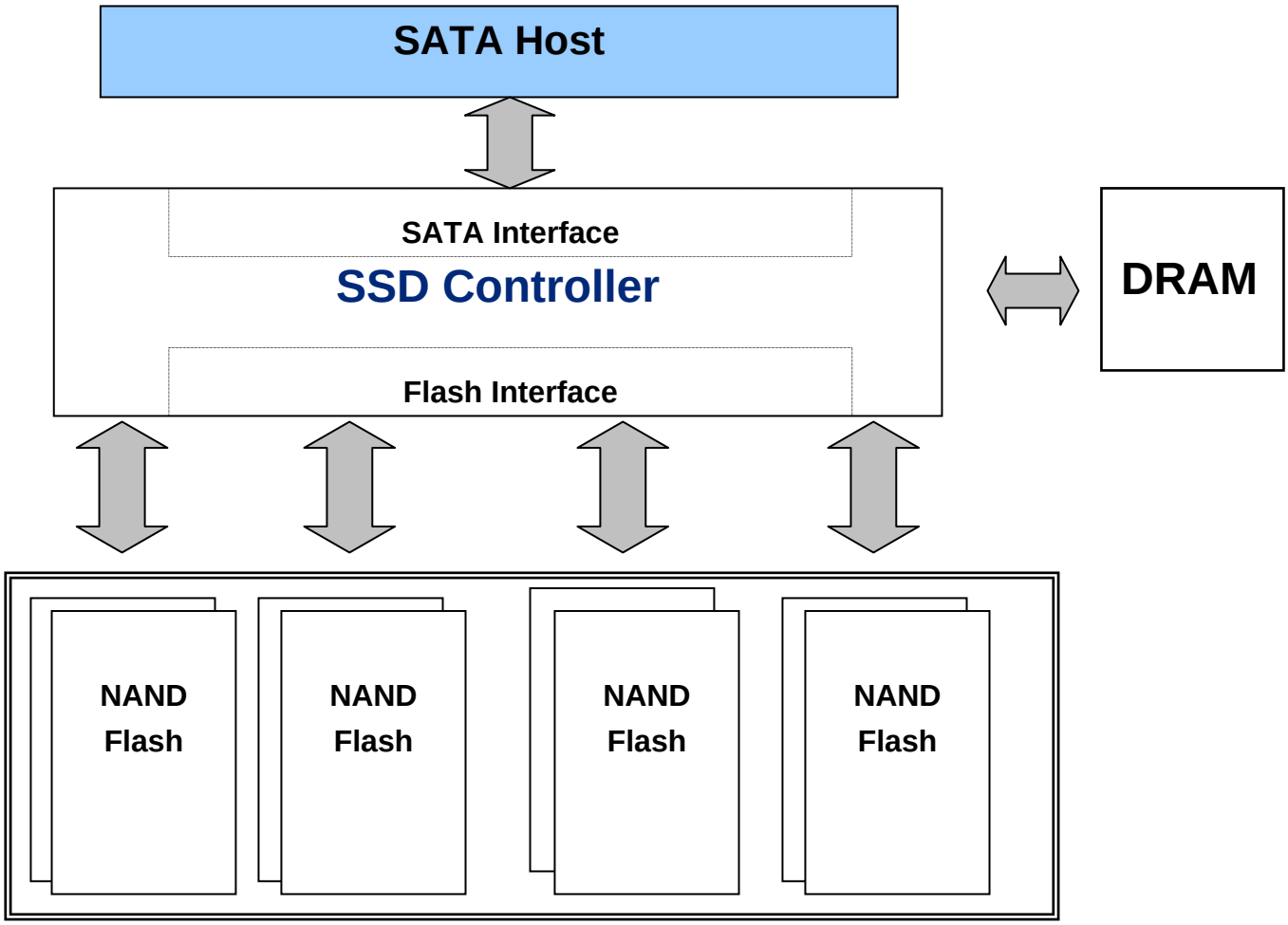
Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name
01	GND	02	A+
03	A-	04	GND
05	B-	06	B+
07	GND	08	3.3V
09	3.3V	10	3.3V
11	GND	12	GND
13	GND	14	5V
15	5V	16	5V
17	GND	18	DAS
19	GND	20	NC
21	NC	22	NC

Pin Layout



Block Diagram



ATA Command Register

The supported ATA command set is shown in the following table

Support ATA/ATAPI Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
READ DMA	C8h	DMA
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	CAh	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Mode Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-In
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data

Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write DMA FUA Ext	3Dh	DMA
Write Multiple Ext	39h	PIO data-out
Write Multiple FUA Ext	CEh	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Other		
Data Set Management	06h	DMA

SMART Data Structure

BYTE	F / V	Description
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-397	F	Reserved
398-399	V	Reserved
400-406	V	'SMI2244'
407-415	X	Vendor specific

416	F	Reserved
417	F	Program/write the strong page only
418-419	V	Number of spare block
420-423	V	Average Erase Count
424-510	X	Vendor specific
511	V	Data structure checksum

F=the content of the byte is fixed and does not change.

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X=the content of the byte is vendor specific and may be fixed or variable.

R=the content of the byte is reserved and shall be zero.

* 4 Byte value : [MSB] [2] [1] [LSB]

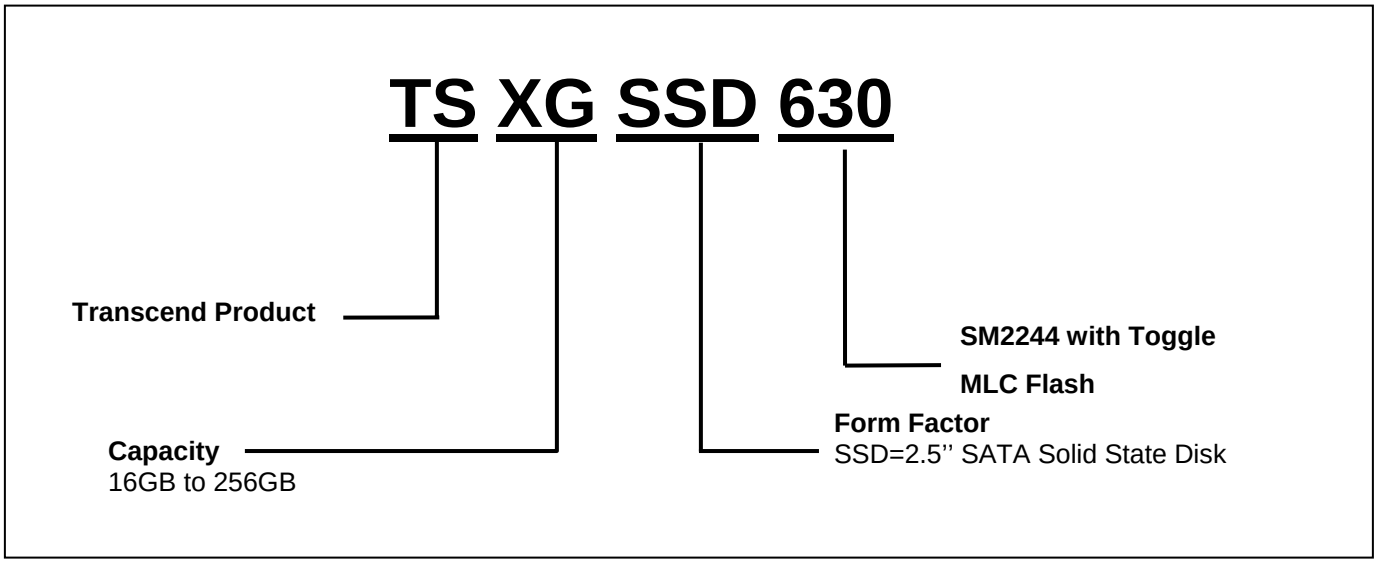
SMART Attributes

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data

Attribute ID (hex)	Raw Attribute Value						Attribute Name
01	MSB	00	00	00	00	00	Read Error Rate
05	LSB	MSB	00	00	00	00	Number of run time bad blocks
09	LSB	-	-	MSB	00	00	Power-On Hours
0C	LSB	MSB	00	00	00	00	Power Cycle Count
C0	LSB	MSB	00	00	00	00	Unexpected Power-off Count
C3	LSB	-	-	MSB	00	00	Hardware ECC recoveries
C4	LSB	-	-	MSB	00	00	Reallocation Event Count
C7	LSB	MSB	00	00	00	00	UltraDMA CRC Error Count
F1	LSB	-	-	MSB	00	00	Total LBA Write Counts (1 Count=32MByte)
F2	LSB	-	-	MSB	00	00	Total LBA Read Counts (1 Count=32MByte)
A0	LSB	-	-	MSB	00	00	Uncorrectable sectors during read/write operations
A1	LSB	MSB	00	00	00	00	Number of valid spare blocks
A3	LSB	MSB	00	00	00	00	Number of initial invalid blocks
A4	LSB	-	-	MSB	00	00	Total erase count
A5	LSB	-	-	MSB	00	00	Maximum erase count
A6	LSB	-	-	MSB	00	00	Minimum Erase count
A7	LSB	-	-	MSB	00	00	Average erase count

Note:
Example1: ID 0x01, only one byte is valid.
Example2: ID 0xA4, 4 bytes is valid.

Ordering Information



The above technical information is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice.

TAIWAN
No.70, XingZhong Rd., NeiHu Dist., Taipei, Taiwan, R.O.C
TEL +886-2-2792-8000
Fax +886-2-2793-2222
E-mail: sales-tw@transcend-info.com
http://tw.transcend-info.com

USA
Los Angeles:
E-mail:sales-us@transcend-info.com
Maryland:
E-mail:sales-us@transcend-info.com
http://www.transcend-info.com
CHINA
E-mail:sales_sh@transcendchina.com
http://cn.transcend-info.com
GERMANY
E-mail:vertrieb-de@transcend-info.com
http://de.transcend-info.com
HONG KONG
E-mail: sales-hk@transcend-info.com
http://hk.transcend-info.com
JAPAN
E-mail: sales-jp@transcend-info.com
http://jp.transcend-info.com
THE NETHERLANDS
E-mail: sales-nl@transcend-info.com
http://nl.transcend-info.com
United Kingdom
E-mail: sales-uk@transcend-info.com
http://uk.transcend-info.com
KOREA
E-mail: sales-kr@transcend-info.com
http://kr.transcend-info.com

Revision History			
Version	**Date**	**Modification Content**	**Modified Page**
V1.0	2012/12/06	Initial Release	
V1.1	2012/12/22	Add TS16GSSD630 info	
V1.2	2013/05/30	Modify LBA to follow IDEMA spec., modify performance	2, 3
V1.3	2013/06/24	Modify TBW value and its remark with according to JEDEC 218&219A standard	4
V1.4	2013/08/06	Add TS96GSSD630 and related info, change pin 18 to DAS	8
V1.5	2013/10/07	Add 9.5mm housing related info, add data retention, add ATA command register info, and modify wordings	1, 2, 4, 5, 7, 8, 11, 12