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ACS-2701A IP67 Waterproof Box PC User Manual

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Aplex Technology, Inc.
15F-1, No.186, Jian Yi Road, Zhonghe District, New Taipei City 235, Taiwan
Tel: 886-2-82262881 Fax: 886-2-82262883 E-mail: aplex@aplex.com.tw URL: www.aplex.com.tw

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Chapter 1

1.1 Features

- Intel Atom Z510 1.1 GHz CPU built-in, upgrade to Z530 1.6 GHz CPU
- Intel US15W chipset
- 1GB DDR2 400 MHz DRAM on board
- Support 1 x 2.5” SATA HDD
- 1 x Mini PCIe slot
- Fanless design
- IP67 Waterproof
- Long life backup battery

1.2 Specifications

System

CPU:

Intel Atom Z510 1.1 GHz CPU built-in, upgrade to Z530 1.6 GHz CPU

Chipset:

Intel US15W chipset

System Memory:

1GB DDR2 400 MHz DRAM on board

Storage:

1 x 2.5” SATA HDD space

1 x CF slot (Internal)

I/O Port: totally IP65 rating connector

1 x RJ45 LAN port

1 x DB15 port for RS-232 and RS-422/485 (Default RS-485)

1 x VGA port

1 x USB port

1 x DC 11~32V

Mechanical

Construction:

Aluminum Dei casting chassis (Top Cover : heat sink design)

Color:

Black

Dimensions:

223(W) x 62(D) x 147(H) mm

Power Supply:

DC 11~32V Input

Environment

Operating temperature:

-20 ~ 60° C

Storage temperature:

-20 ~ 70° C

Relative humidity:

10~90% @ 40° C non-condensing

Certificate

CE/FCC Class A

1.3 Dimensions

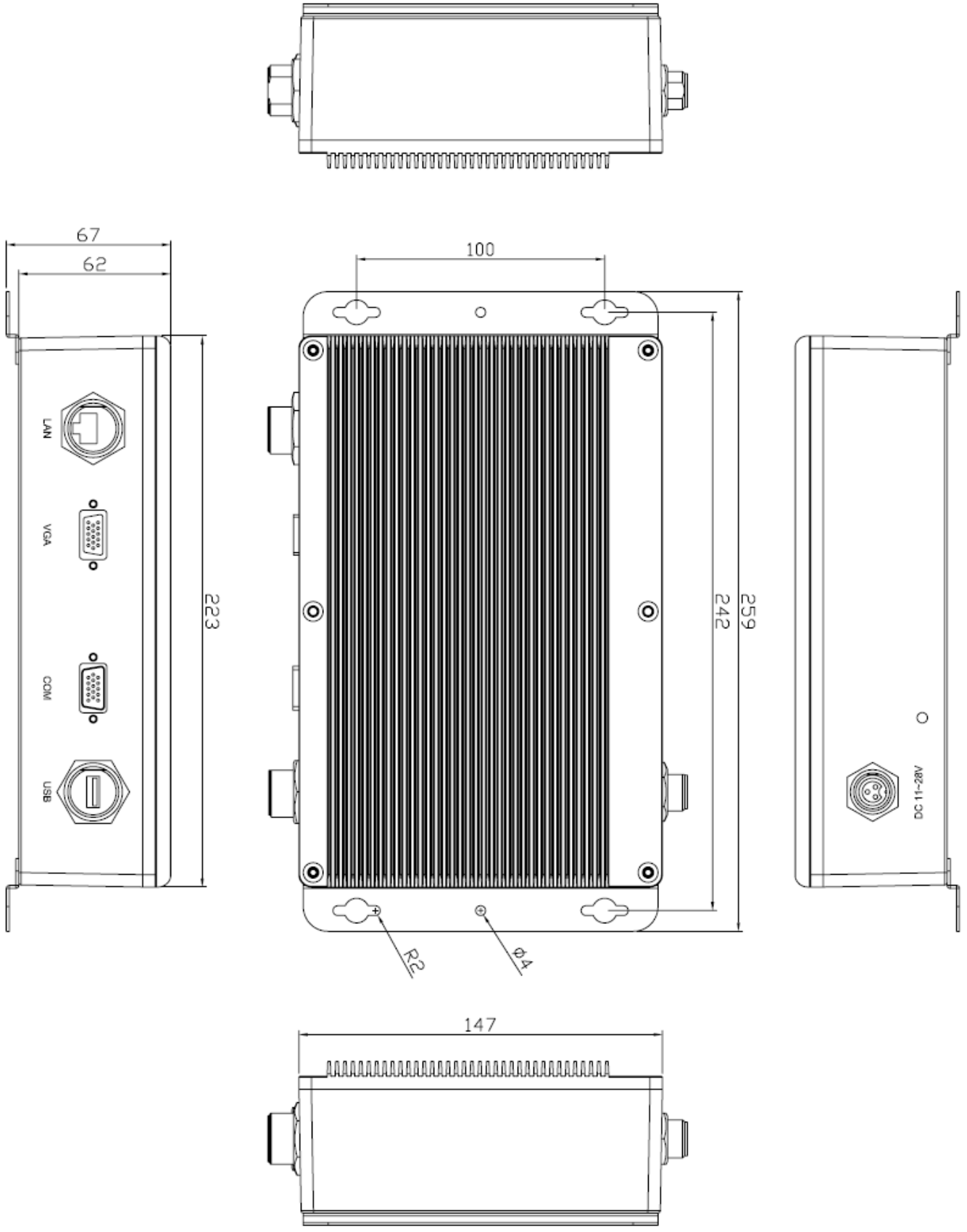


Figure 1.1: Dimensions of the ACS-2701A

1.4 Brief Description of the ACS-2701A

The ACS-2701A is a Fanless IP67 Waterproof Solution and ultra-compact standalone embedded controller, powered by onboard Intel Atom Z510 1.1GHz, and supporting 1 x USB Port, 1 x DB 15 Port for RS-232 and RS-485, 1 x VGA Port , 1 x LAN Port and totally IP67 rating connectors. It is ideal for Industrial Automation & Outdoor Automation, etc. and running factory operations from small visual interface and maintenance applications to large control process applications. The ACS-2701A works very well along with any of our Display Monitor series. It absolutely can provide an easy way to perform control and field maintenance. It comes with a DC11~32V wide-ranging power input.

Figure 1.2: Front View of ACS-2701A

Chapter 2 Hardware Installation

2.1 Mainboard

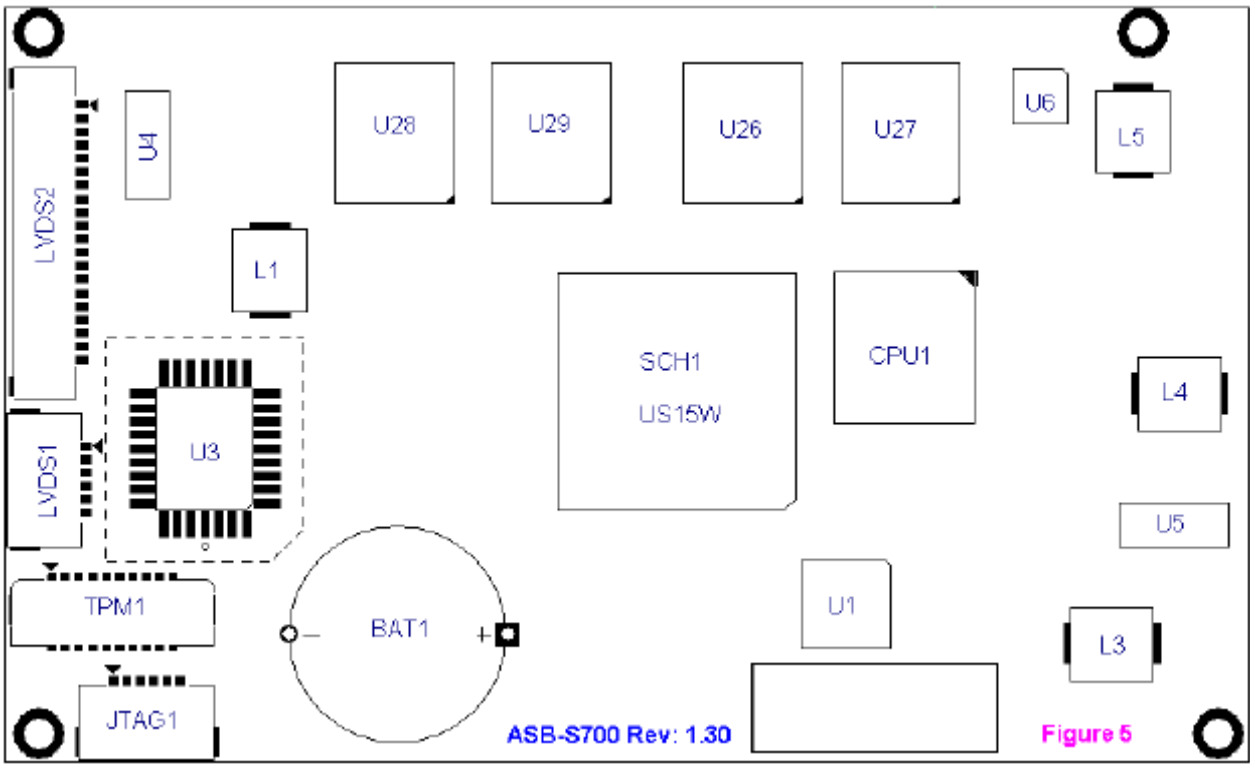


Figure 1.3: ASB- S700 Top- view connectors

2.1.1 JTAG1

JTAG1 was dedicated debug purpose for manufacturer only, users prohibited.

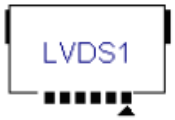
2.1.2 TPM1

TPM1 was dedicated debug purpose for manufacturer only, users prohibited.

2.1.3 LVDS1

LVDS1 is the power supply of LVDS screen backlight and control-board interface, using HIROSE's DF14A-6P-1.25H connector or other company's compatible connector. The pins are defined as follows.

Pin Number	Signal	Description
1	VCC	Default 12V (5V as option by requested OEM/ ODM order)
2	VCC	Default 12V (5V as option by requested OEM/ ODM order)
3	Ground	Signal Ground
4	Ground	Signal Ground
5	BKLTON	backlight turn- on
6	BKLTCTL	backlight brightness control



- Note 1: The interface number identifies the edge of the triangle is the Pin 1 position, the same below.
- Note 2: ASB-S700 Rev: 1.20, Rev: 1.30 and later version, VCC of LVDS1 default is12V.

2.1.4 LVDS2

LVDS2 is the LVDS screen signal interface connectors, using HIROSE's DF14A-20P-1.25H connector or other company's compatible connector. The pins are defined as follows.

Pin Number	Signal	Description
1	VCC_LCD	Default 3.3V (5V option by requested OEM/ ODM order)
2	VCC_LCD	
3	Ground	Signal Ground
4	Ground	Signal Ground
5	D0-	LVDS_0 negative differential signal output
6	D0+	LVDS_0 positive differential signal output
7	Ground	Signal Ground
8	D1-	LVDS_1 negative differential signal output
9	D1+	LVDS_1 positive differential signal output
10	Ground	Signal Ground
11	D2-	LVDS_2 negative differential signal output
12	D2+	LVDS_2 positive differential signal output
13	Ground	Signal Ground
14	CLK-	LVDS negative differential clock signal output
15	CLK+	LVDS positive differential clock signal output
16	Ground	Signal Ground
17	D3-	LVDS_3 negative differential signal output
18	D3+	LVDS_3 positive differential signal output
19	Ground	Signal Ground
20	RSV	Reserved

- Note 3: ASB-S700 Rev: 1.20, Rev: 1.30 and later version, VCC of LVDS2 default is3.3V.

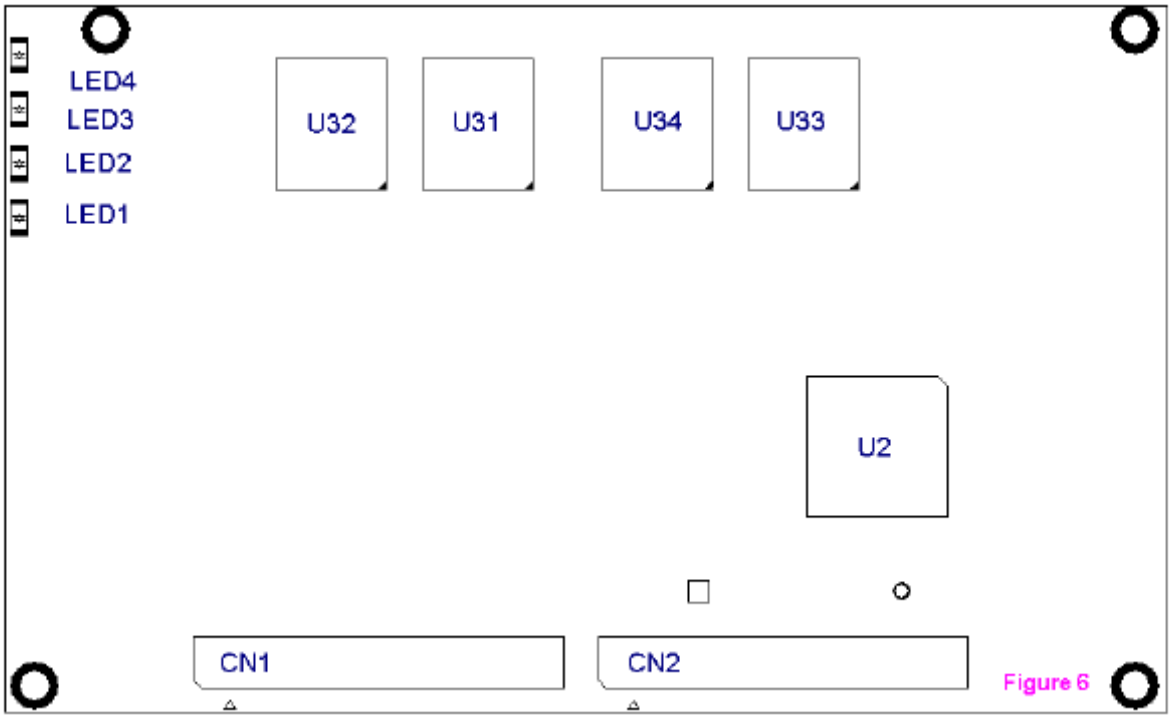
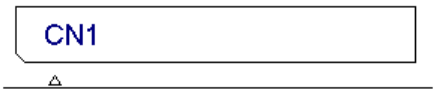


Figure 1.4: ASB- S700 Bottom- view LED and Connectors

2.1.5 LED1~ LED4

There are 4x LEDs
LED1: Main power indicator。
LED2: IDE/ HDD device indicator。
LED3: DEBUG LED， programmable by manufacturer。
LED4: DEBUG LED， programmable by manufacturer。

2.1.6 CN1 pins- assignment



Pin Number	Signal Description	Pin Number	Signal Description
1	12V_S5	2	GND (Ground)
3	12V_S5	4	PCIE_RXN
5	12V_S5	6	PCIE_RXP
7	12V_S5	8	NC (No Connect)
9	12V_S5	10	CLK_100M_PE1N
11	12V_S5	12	CLK_100M_PE1P
13	GND (Ground)	14	GND (Ground)
15	GND (Ground)	16	PCIE1_TXN
17	3P3V_S5	18	PCIE1_TXP
19	3P3V_S5	20	GND (Ground)
21	3P3V_S5	22	5V_S0
23	3P3V_S5	24	5V_S0
25	GND (Ground)	26	5V_S0
27	GND (Ground)	28	5V_S0
29	5V_S0	30	GND (Ground)
31	5V_S0	32	SDIO_D7
33	5V_S0	34	SDIO_D6
35	5V_S0	36	SCH_GPIO2
37	IDE1_66DET	38	SCH_GPIOSUS0
39	GND (Ground)	40	PCIE_PME#
41	IDE_D7	42	SCH_GPIO8
43	IDE_D8	44	3P3V_S0
45	IDE_D6	46	3P3V_S0
47	IDE_D9	48	3P3V_S0
49	IDE_D5	50	3P3V_S0
51	IDE_D10	52	3P3V_S0
53	IDE_D4	54	3P3V_S0
55	IDE_D11	56	GND (Ground)
57	IDE_D3	58	PCIE2_TXP
59	IDE_D12	60	PCIE2_TXN
61	IDE_D2	62	GND (Ground)
63	IDE_D13	64	SDIO_D5
65	IDE_D1	66	SDIO_D4
67	IDE_D14	68	SDIO_D3
69	IDE_D0	70	SDIO_D2
71	IDE_D15	72	SDIO_D1
73	GND (Ground)	74	SDIO_D0
75	IDE_DREQ	76	SDIO_CLK

77	IDE_IOW#	78	SDIO_CMD
79	IDE_IOR#	80	GND (Ground)
81	IDE_IORDY#	82	PCIE_CLKP
83	IDE_DACK#	84	PCIE_CLKN
85	IDE_IRQ	86	GND (Ground)
87	IDE_DA1	88	PCIE2_RXP
89	IDE_DA0	90	PCIE2_RXN
91	IDE_DA2	92	SCH_GPIO6
93	IDE_CS1#	94	SDIO_CD#
95	IDE_CS3#	96	SDIO_WP
97	IDE_ACT#	98	SLP_S3#
99	GND (Ground)	100	PSON#
101	NPTH1 as guide-socket as foolproof	102	NTTH2 as guide-socket as foolproof

- Note 4: SB-S700 CN1 is defined and ready to adapt to CN3 onto the baseboard.

Please refer to the relevant bus specifications from INTEL Design Guidelines. As they are involved the dedicated bus signals (such as IDE, PCIE, LPC, USB, SDVO, HAD, SDIO, SMB, etc.) specific roles and design requirements.

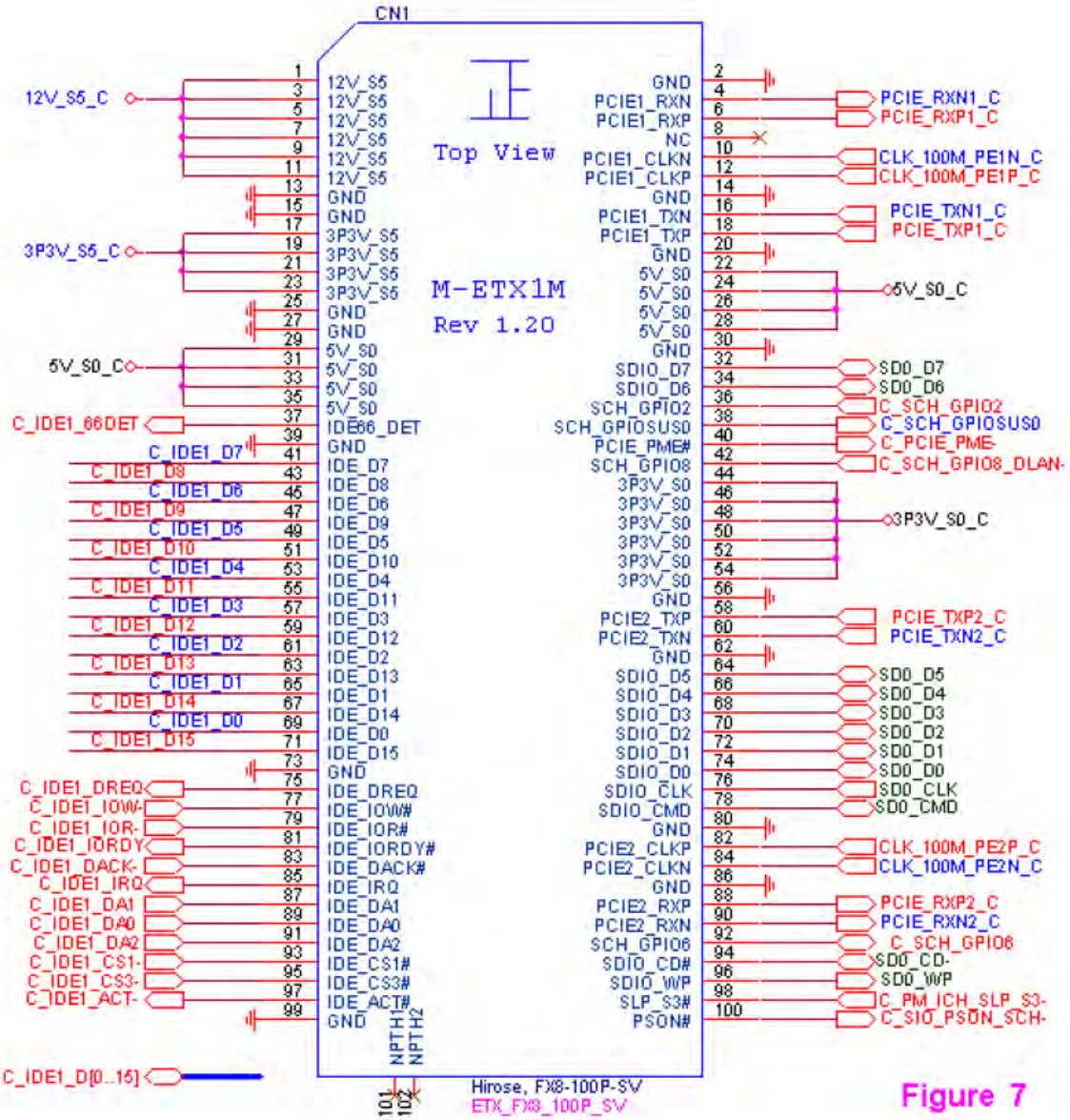


Figure 7

2.1.6.1 NC- Pin

Means non- connected pin, part of the pins of CN1/ CN2 (left or right) are not connected for reservation

Purpose

2.1.6.2 RSV- Pin

This pin was reserved for specific function and definition maybe different from CN1 or CN3 (top or down)

2.1.6.3 GND ground pin

2.1.6.4 Power Supply Source Class

There are four pins for power supply sources on CN1:

12V_S5, is defined for 12V standby power, connected Pin 1, 3, 5, 7, 9, 11 of total six pins, can secure transmission current up to 2.4 Amp.

3P3V_S5, is defined for 3.3V standby power, connected Pin 17, 19, 21, 23 of total four pins, can secure transmission current up to 1.6 Amp.

3P3V_S0, is defined for 3.3V system power source, connected Pin 44, 46, 48, 50, 52, 54 of total six pins, can secure transmission current up to 2.4Amp.

5V_S0, is defined for 5V system power source, connected Pin 22, 24, 26, 28, 29, 31, 33, 35 of total eight pins, can secure transmission current up to 3.2 Amp.

2.1.6.5 IDE bus signal

Pin 37 and the odd pin- number in between #41 ~ # 97 are defined for IDE bus signals.

2.1.6.6 PCIE (PCI-Express) bus- signals

ASB-S700 supports two PCI-E 1x bus. (1x lanes)

Pin 4, 6 are defined for the PCIE1 differential negative as positive input signal, Pin16, 18 are defined for the PCIE1 differential negative as positive output signal, and Pin10, 12 are defined for the differential negative as the clockwise output signal.

Pin 58, 60 are defined for the PCIE2 differential positive as negative output signal, Pin88, 90 are defined for the PCIE2 differential positive as negative input signals, Pin82, 84 are defined for the differential positive as counterclockwise output signal

2.1.6.7 SDIO bus signal

Pin 68, 70, 72, 74, 78, 94, 96 are for the SDIO bus signals, can support 4 bit SDIO devices.

Pin 32, 34, 64, 66 are reserved and malfunction.

2.1.6.8 Other Signals

Pin36, US15W's GPIO3 signal (the initial status is defined as the output);

Pin38, US15W's GPIOSUS0 signal (the initial status is defined as the input);

Pin40, PCIE_PME # signal, the external device wake-up signal (#, said active-low);

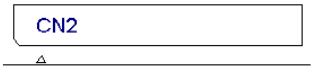
Pin42, US15W's GPIO8 signal; (can be defined for LAN disable signal)

Pin92, US15W the GPIO6 signal;

Pin98, SCH_SLP3 # signal, control system power supply;

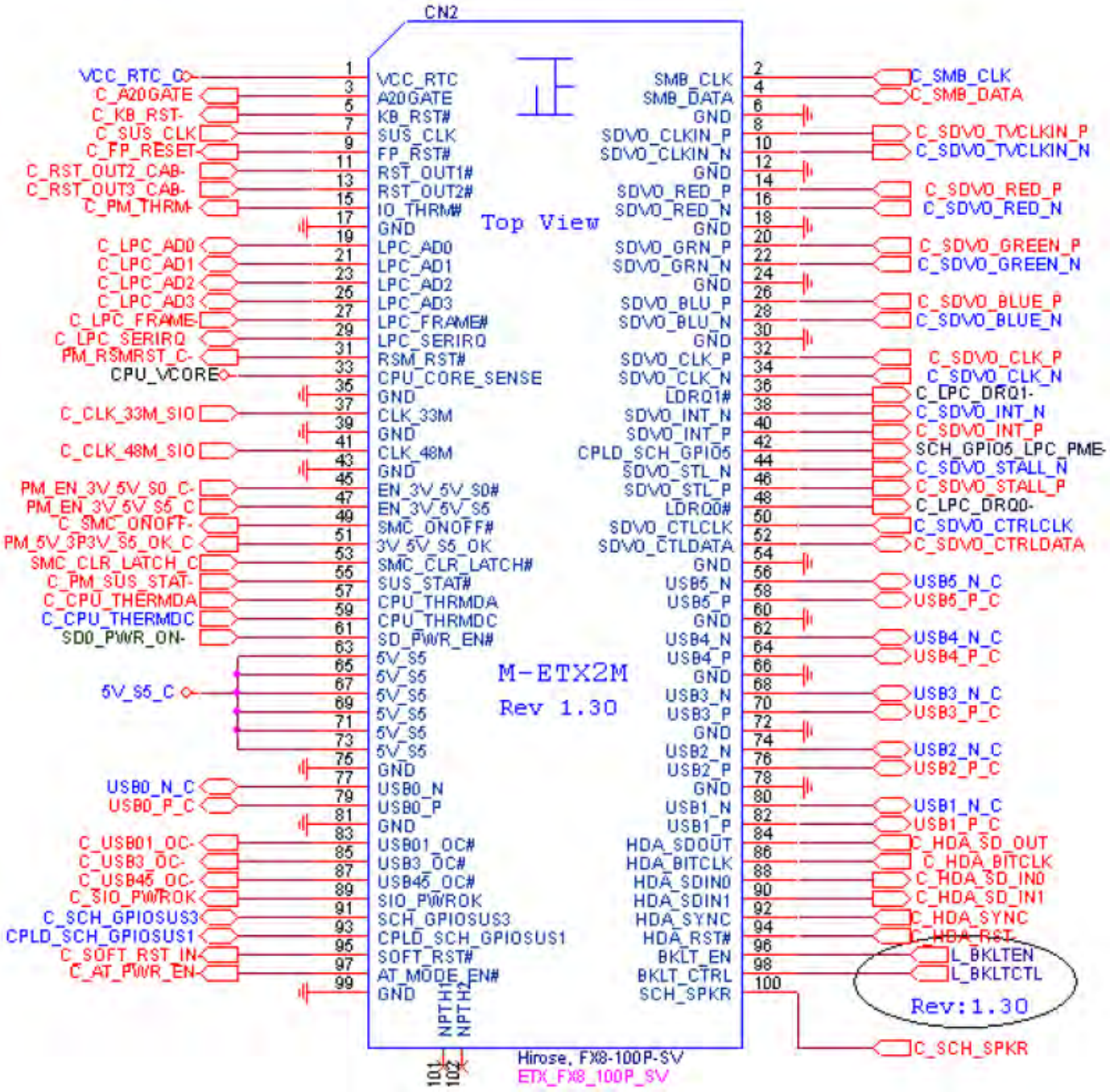
Pin100, SIO_PSON # signal, SIO transferred switching ON/ OFF power supply signal.

2.1.7 CN2 pins- assignment (R1.30)



Pin Number	Signal Description	Pin Number	Signal Description
1	VCC_RTC	2	SMB_CLK
3	A20GATE	4	SMB_DATA
5	KB_RST#	6	GND (Ground)
7	SUS_CLK	8	SDVO_CLKIN_P
9	FP_RST#	10	SDVO_CLKIN_N
11	RST_OUT1#	12	GND (Ground)
13	RST_OUT2#	14	SDVO_RED_P
15	IO_THRM#	16	SDVO_RED_N
17	GND (Ground)	18	GND (Ground)
19	LPC_AD0	20	SDVO_GRN_P
21	LPC_AD1	22	SDVO_GRN_N
23	LPC_AD2	24	GND (Ground)
25	LPC_AD3	26	SDVO_BLU_P
27	LPC_FRAME#	28	SDVO_BLU_N
29	LPC_SERIRQ	30	GND (Ground)
31	RSM_RST#	32	SDVO_CLK_P
33	CPU_CORE_SENSE	34	SDVO_CLK_N
35	GND (Ground)	36	LDRQ1#
37	CLK_33M	38	SDVO_INT_N
39	GND (Ground)	40	SDVO_INT_P
41	CLK_48M	42	CPLD_SCH_GPIO5
43	GND (Ground)	44	SDVO_STL_N
45	EN_3V_5V_S0#	46	SDVO_STL_P
47	EN_3V_5V_S5	48	LDRQ0#
49	SMC_ONOFF#	50	SDVO_CTLCLK
51	3V_5V_S5_OK	52	SDVO_CTLDATA
53	SMC_CLR_LATCH#	54	GND (Ground)
55	SUS_STAT#	56	USB5_N
57	CPU_THRMDA	58	USB5_P
59	CPU_THRMDC	60	GND (Ground)
61	SD_PWR_EN#	62	USB4_N
63	5V_S5	64	USB4_P
65	5V_S5	66	GND (Ground)
67	5V_S5	68	USB3_N
69	5V_S5	70	USB3_P
71	5V_S5	72	GND (Ground)
73	5V_S5	74	USB2_N
75	GND (Ground)	76	USB2_P
77	USB0_N	78	GND (Ground)
79	USB0_P	80	USB1_N
81	GND (Ground)	82	USB1_P
83	USB01_OC#	84	HDA_SDOUT
85	USB3_OC#	86	HDA_BITCLK
87	USB45_OC#	88	HAD_SDIN0
89	SIO_PWROK	90	HDA_SDIN1
91	SCH_GPIOSUS3	92	HAD_SYNC
93	CPLD_SCH_GPIOSUS1	94	HDA_RST#
95	SOFT_RST#	96	BKLT_EN
97	AT_MODE_EN#	98	BKLT_CTRL
99	GND	100	SCH_SPKR
101	NPTH1 as guide-socket as foolproof	102	NTTH2 as guide-socket as foolproof

- Note 5: ASB-S700 defined CN2 and ready to adapt to CN4 onto the baseboard.



2.1.7.1 NC- Pin

Means non- connected pin, part of the pins of CN1/ CN2 (left or right) are not connected for reservation
purpose.

RSV- Pin
This pin was reserved for specific function and definition maybe different from CN1 or CN3 (top or down)

GND ground pin

2.1.7.2 Power Supply Pin

CN2, CN4 defined two kinds of power supply sources.

VCC_RTC, is defined for the Real-Time-Clock power supply, ASB-S700 is equipped with a lithium battery (CR2032) also the onboard battery is also for the baseboard used.

5V_S5, is defined for 5V Standby power source, connected Pin63, 65, 67, 69, 71, 73 of total of six pins, can secure transmission current up to 2.4 Amp.

2.1.7.3 LPC Bus Signal

Pin36, 48 and odd-number of pin 19 ~ 29 are defined for LPC Bus signals.

2.1.7.4 USB Bus Signal

Pin77, 79, Pin56, 58, Pin62, 64, Pin68, 70, Pin74, 76, Pin80, 82, are defined set of differential pairs of negative as positive signals of USB. Pin83, 85, 87 are defined as over-current protection signal for relevant USB ports.

2.1.7.5 SMB Bus Signal

Pin2, 4 are defined for the SMB Bus signals

2.1.7.6 SDVO Bus Signal

The even-number of Pin8 ~ 52 are defined for SDVO Bus signals

2.1.7.7 HDA Bus Signal

The even-number of Pin84 ~ 94 are defined for High Definition Audio Bus signals of Intel.

2.1.7.8 Clock Signals

Pin7 is defined for 32.768 KHz clock signal, output from CPU board, core-module of mini-Express.
Pin37 is defined for the 33MHz clock signal, output from CPU board, core-module of mini-Express.
Pin41 is defined for the 48MHz clock signal, output from CPU board, core-module of mini-Express.

2.1.7.9 Other Signals

Pin3, A20GATE, is defined for A20 GATE signal as issued by SIO. (Serial Input/ Output)
Pin5, KB_RST #, is defined for Keyboard Reset as issued by SIO. (#, said active-low);
Pin9, FP_RST #, is defined as forced Reset signal from external input;
Pin11, RST_OUT1 #, CPU board, core-module send-out reset signal #1 to the adapted IO baseboard.
Pin13, RST_OUT2 #, CPU board, core-module send-out reset signal #2 to the adapted IO baseboard.
Pin15, IO_THRM #, IO baseboard send the system thermal- overheat signal to CPU board.
Pin31, RSM_RST #, IO baseboard send system reboot ready signal to CPU board.;
Pin33, CPU_CORE_SENSE, CPU core- power supply voltage detection;
Pin42, multiplexed signal can be used for LPC_PME # and GPIO;
Pin45, EN_3V_5V_S0 #, CPU board send the main power system signal to IO baseboard for operating

Pin47, EN_3V_5V_S5, CPU board send an auxiliary power supply signal to IO baseboard for operating.
Pin49, SMC_ONOFF #, IO baseboard send to CPU board to issue a system ON/ OFF signal;
Pin51, 3V_5V_S5_OK, IO baseboard issued confirmed auxiliary power OK signal to CPU board;
Pin53, SMC_LATCH #, CPU board sent disable system signal to the IO baseboard;
Pin57, CPU_THERMDA, Defined the thermal diode positive signal to CPU board;
Pin59, CPU_THERMDC, Defined the thermal diode negative signal to CPU board;
Pin89, SIO_PWROK, IO baseboard send to the power OK signal to CPU board;
Pin91, USB2_CLIENT_EN, USB2_CLIENT signal enable, but also can be defined as GPIO;
Pin93, from the US15W access via CPLD out as defined GPIO;
Pin95, Software Reset signal, active low;
Pin97, AT Power Mode allows signal, active low;
Pin100, SCH_SPKR, CPU board sent to the buzzer signal- sound to IO baseboard

2.1.7.10 LVDS panel backlight signal

The main different functions of Rev: 1.20 version and Rev: 1.30 version is the CN2 added LVDS backlight
control screen signals.
Pin 96 L_BKLEN, is defined for Backlight start signal;
Pin 98 L_BKLCTRL, is defined for backlight brightness control signal.

2.2 Component Locations

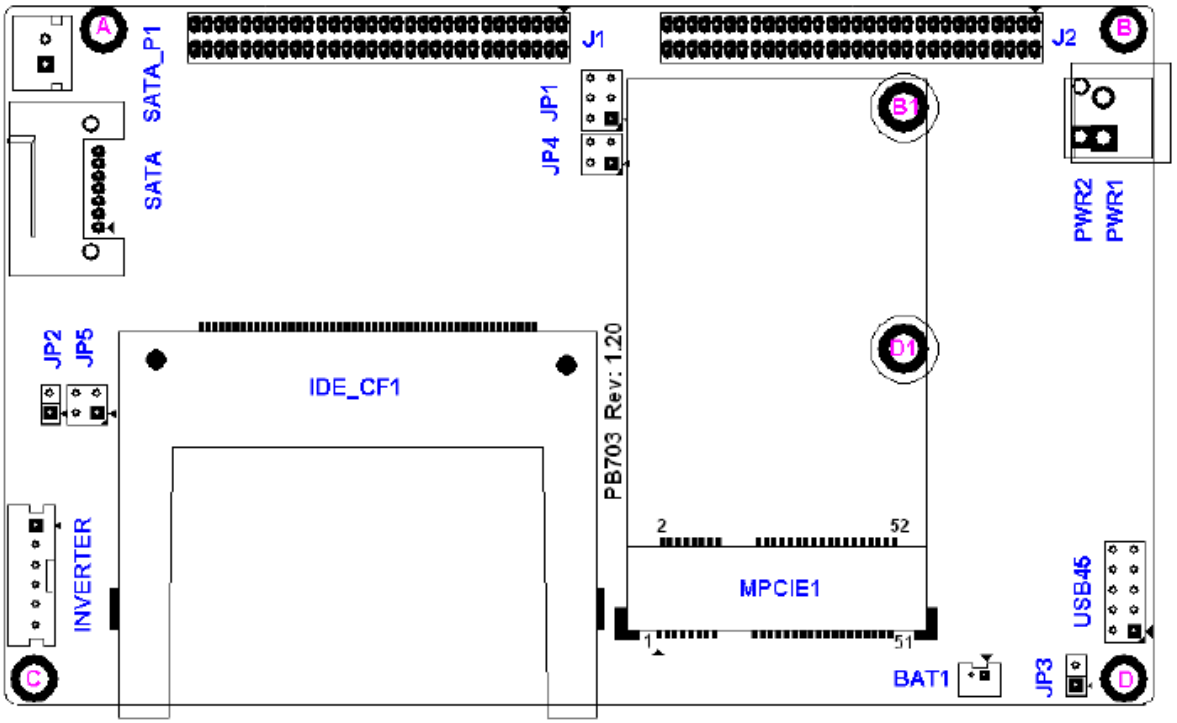


Figure 1.5: PB-703 Baseboard Overview

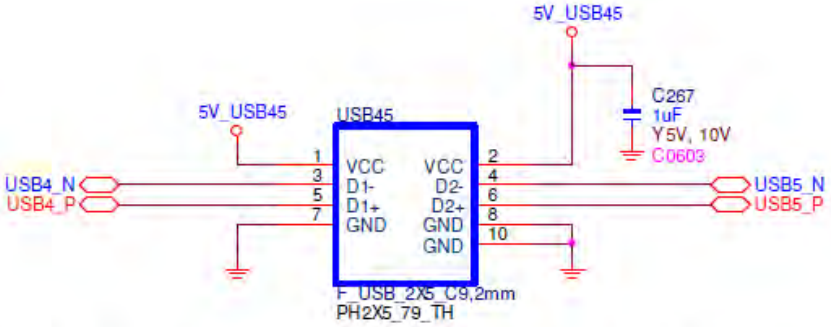
2.2.1 PWR1/PWR2

The power input of PCB was co-designed with PWR1or PWR2 for pre-selection。

PWR1 will use CJT brand like A3963WV-2P type connectors，PWR2 may use DINKLE brand like DT-126RP-02P type connectors。PWR1/PWR2 are different housing design but same pin defined：

Pin #	Pin Assignment
1	VCC (+12V +/- 10%)
2	Ground

2.2.2 USB4/5



Pitch2.0mm，2× 5Pins header including 2x USB signals，pin- defined as follow：

Pin #	Pin Assignment
1	VCC
2	VCC
3	D1+
4	D2-
5	D1-
6	D2+
7	GND
8	GND
9	NC
10	GND

2.2.3 JP3

JP3 is designed for auto-on switch jumper with 2xPin-header as pitch 2.0mm type.

JP3 defaulted with closed jumper, system will be on when DC power input.

If JP3is open jumper, system power-on will be controlled by firmware of ASB-S700.

2.2.4 BAT1

Wafer 2x pins with brand CJT-A1251WV-2P type connector with pitch1.25mm for real-time clock battery input

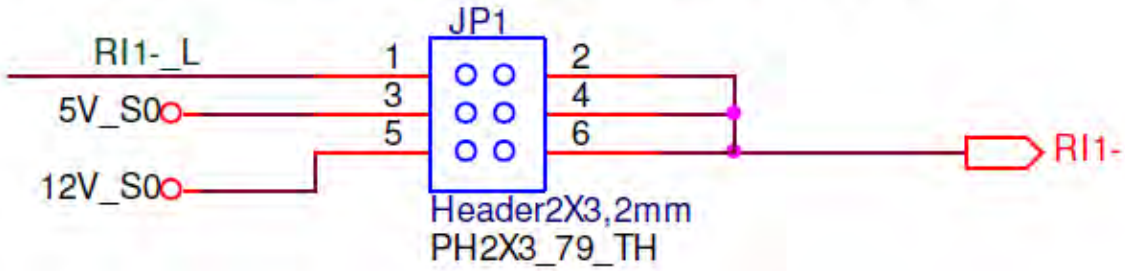
Pin #	Pin Assignment
1	VCC（over 3V）
2	Ground

2.2.5 MPCIE1 [mini- PCI express]

Mini PCI Express slot for full-/ half- size add-in card，initial designed for full-size mPCIe could be fixed on A1 and B1，optional designed for half-size mPCIe could be fixed on C1 and D1

2.2.6 JP1

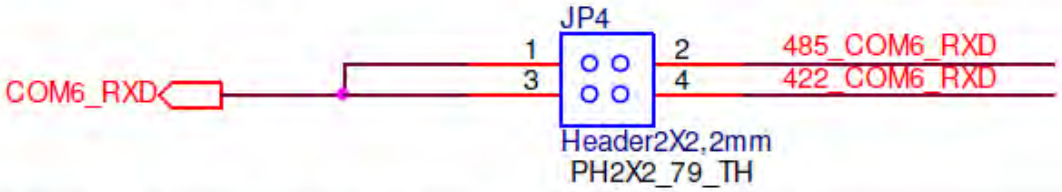
Pitch 2.0mm，2x 3 Pin-header，COM1 Ring Indicator as signal selection



JUMPER	COM1 DB9- Pin# 9 defined
1-2	RS232 port standard RI# defined
3-4	5V power
5-6	12V power

2.2.7 JP4

Pitch 2.0mm，2x2 Pin- header，RS485/RS422 selection mode。
COM6 is designed for RS485/RS422 port，using JP4 pre-select mode。
COM6 signals defined for RS485/RS422 within J1 port #7-8-9-10。



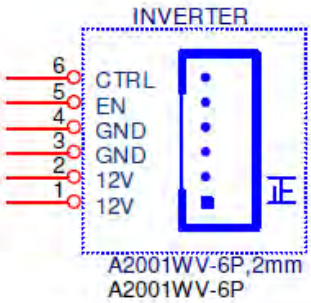
JUMPER	COM6 RS485/RS422
1-2	RS485
3-4	RS422

2.2.8 IDE_CF1

IDE_CF1 designed as Compact Flash slot，support Type Ⅰ、Type Ⅱ CF card。
CF slot working voltage could be select on 3.3V or 5V，PB-703 is default 3.3V operation。
Note 6：for optional 5V supported CF slot, it will be ODM project requested for new PCB design。

2.2.9 INVERTER

Reserved LCD backlight control power port with CJT brand type A2001WV-6P-1 connector with 6x pins header, 2mm pitch as pin defined as follow：



Pin #	Pin Assignment
1	12V
2	12V
3	Ground
4	Ground
5	BKLT_EN
6	Brightness_CTRL

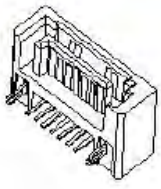
2.2.10 JP2

Jumper selection for LVDS backlight brightness control with pitch 2.0 mm, 2xPins header

Mode	LVDS backlight brightness control selection
Open	Backlight brightness control by PWM mode.
Close	Backlight brightness control DC voltage mode (default)

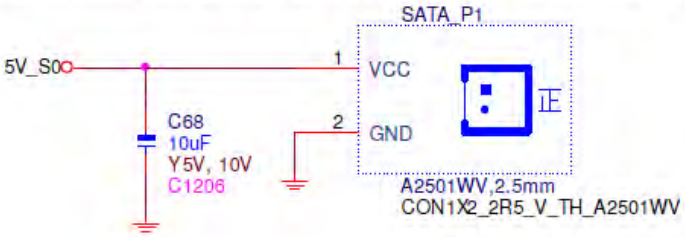
2.2.11 SATA

The 7Pin SATA port using FOXCONN brand LD1707V-S31B1 type connector, it support lockable cable of SATA
Note 7：Our SATA is shared-IDE designed with IDE_CF1 slot, mater and slave mode could be selected by 2.13



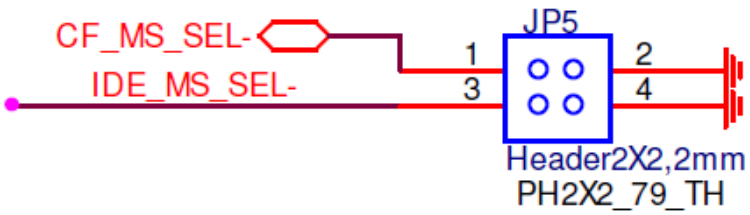
2.2.12 SATA_P1

SATA HDD power port for 5V input, using CJT brand A2501WV-2P type connector and its pin defined as follow：



2.2.13 JP5

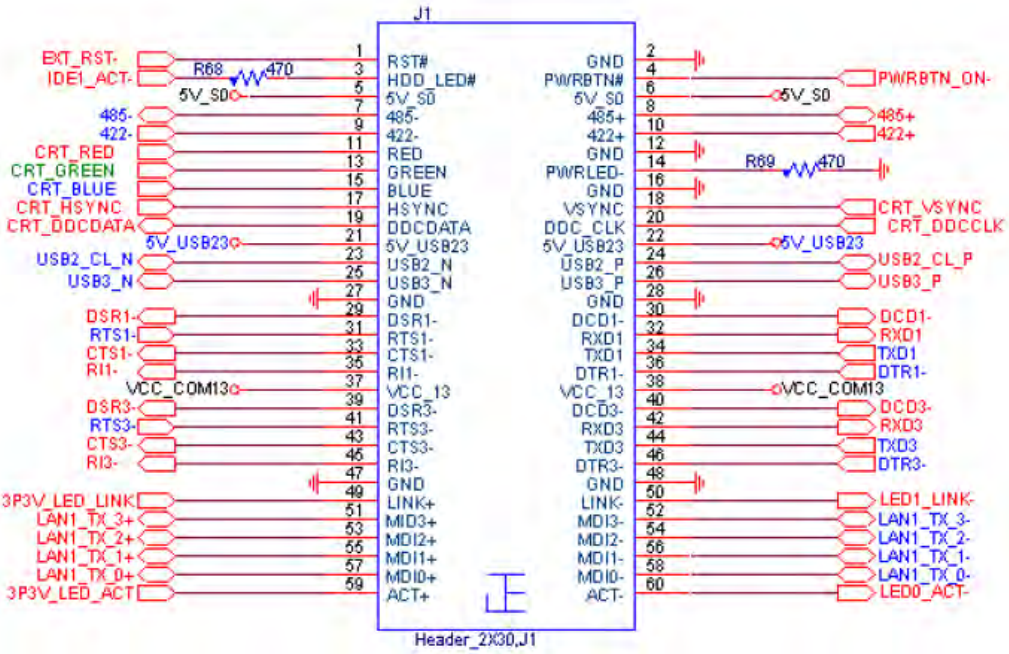
As jumper to select master of shared-IDE CF card vs. SATA HDD



JUMPER	CF card、SATA HDD master/ slave mode setting
1-2	CF card as master mode (shared- IDE)
3-4	SATA HDD as master m ode (shared- IDE)

2.2.14 J1 Port

J1 port is using FJY brand FJ24D01-60-C-1-5/2.5 type pin-header as multi- functions signals with its pins defined as follow：

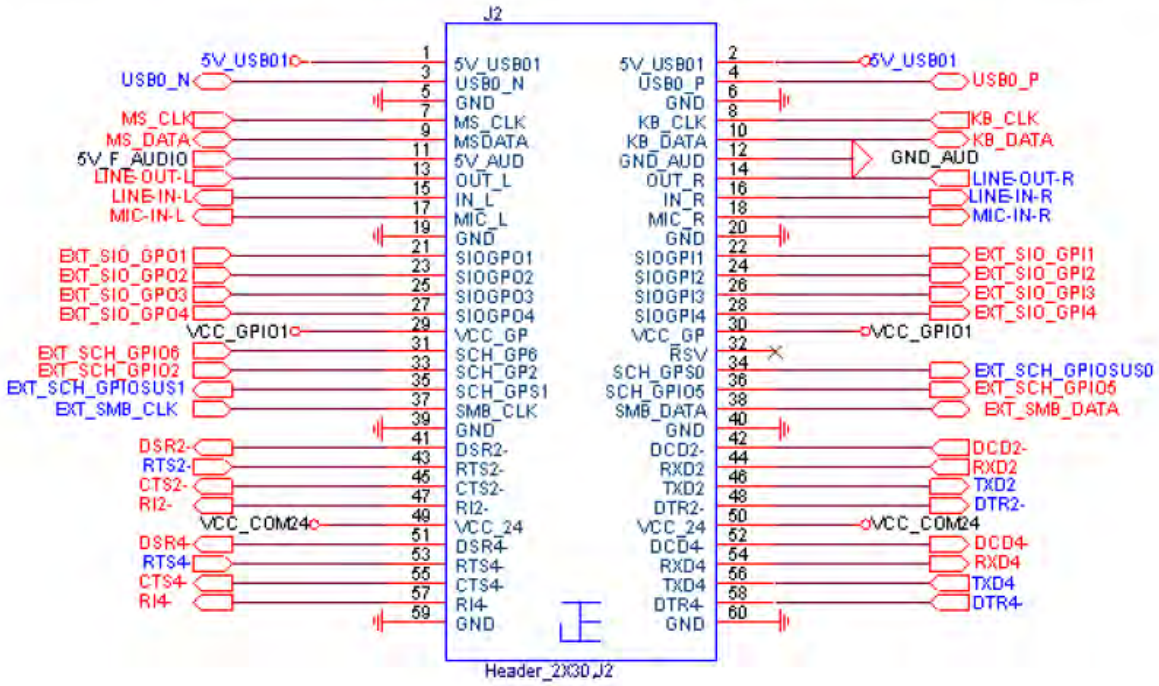


J1, pins defined table：

Pin#	Pin assignment	defined	Pin#	Pin assignment	defined
1	EXT_RST-	Reset	2	GND	
3	IDE1_ACT-		4	PWRBTN_ON-	Power On
5	5V_S0		6	5V_S0	
7	485-	RS485	8	485+	RS485
9	422-	RS422	10	422+	RS422
11	CRT_RED	VGA	12	GND	
13	CRT_GREEN		14	GND	
15	CRT_BLUE		16	GND	
17	CRT_HSYNC		18	CRT_VSYNC	VGA
19	CRT_DDCDATA		20	CRT_DDCCLK	
21	5V_USB23		22	5V_USB23	
23	USB2_CL_N	USB2	24	USB2_CL_P	USB2
25	USB3_N	USB3	26	USB3_P	USB3
27	GND		28	GND	
29	DSR1-	COM1 (RS232)	30	DCD1-	COM1
31	RTS1-		32	RXD1	
33	CTS1-		34	TXD1	
35	RI1-		36	DTR1-	
37	VCC_COM13		38	VCC_COM13	
39	DSR3-	COM3	40	DCD3-	COM3
41	RTS3-		42	RXD3	
43	CTS3-		44	TXD3	
45	RI3-		46	DTR3-	
47	GND		48	GND	
49	3P3V_LED_LINK	LAN	50	LED1_LINK-	LAN
51	LAN1_TX_3+		52	LAN1_TX_3-	
53	LAN1_TX_2+		54	LAN1_TX_2-	
55	LAN1_TX_1+		56	LAN1_TX_1-	
57	LAN1_TX_0+		58	LAN1_TX_0-	
59	3P3V_LED_ACT		60	LED0_ACT-	

2.2.15 J2 port

J2 port using FJY brand FJ24D01-60-C-1-5/2.5 type pin-header as multi- functions signals with its pins defined as follow：



J2, pins defined table：

Pin #	Pin assignment	defined	Pin #	Pin assignment	defined
1	5V_USB01		2	5V_USB01	
3	USB0_N	USB0	4	USB0_P	USB0
5	GND		6	GND	
7	MS_CLK	PS/2 (MOUSE)	8	KB_CLK	PS/2 (KEYBOARD)
9	MS_DATA		10	KB_DATA	
11	5V_F_AUDIO	AUDIO	12	GND_AUD	AUDIO
13	LINE-OUT-L		14	LINE-OUT-R	
15	LINE-IN-L		16	LINE-IN-R	
17	MIC-IN-L		18	MIC-IN-R	
19	GND		20	GND	
21	EXT_SIO_GPO1	GPO	22	EXT_SIO_GPI1	GPI
23	EXT_SIO_GPO2		24	EXT_SIO_GPI2	
25	EXT_SIO_GPO3		26	EXT_SIO_GPI3	
27	EXT_SIO_GPO4		28	EXT_SIO_GPI4	
29	VCC_GPIO1		30	VCC_GPIO1	
31	EXT_SCH_GPIO6	GPIO	32	NC	
33	EXT_SCH_GPIO2		34	EXT_SCH_GPIOSUS0	GPIO
35	EXT_SCH_GPIOSUS1		36	EXT_SCH_GPIO5	
37	EXT_SMB_CLK		38	EXT_SMB_DATA	
39	GND		40	GND	
41	DSR2-	COM2	42	DCD2-	COM2
43	RTS2-		44	RXD2	
45	CTS2-		46	TXD2	
47	RI2-		48	DTR2-	
49	VCC_COM24		50	VCC_COM24	
51	DSR4-	COM4	52	DCD4-	COM4
53	RTS4-		54	RXD4	
55	CTS4-		56	TXD4	
57	RI4-		58	DTR4-	
59	GND		60	GND	

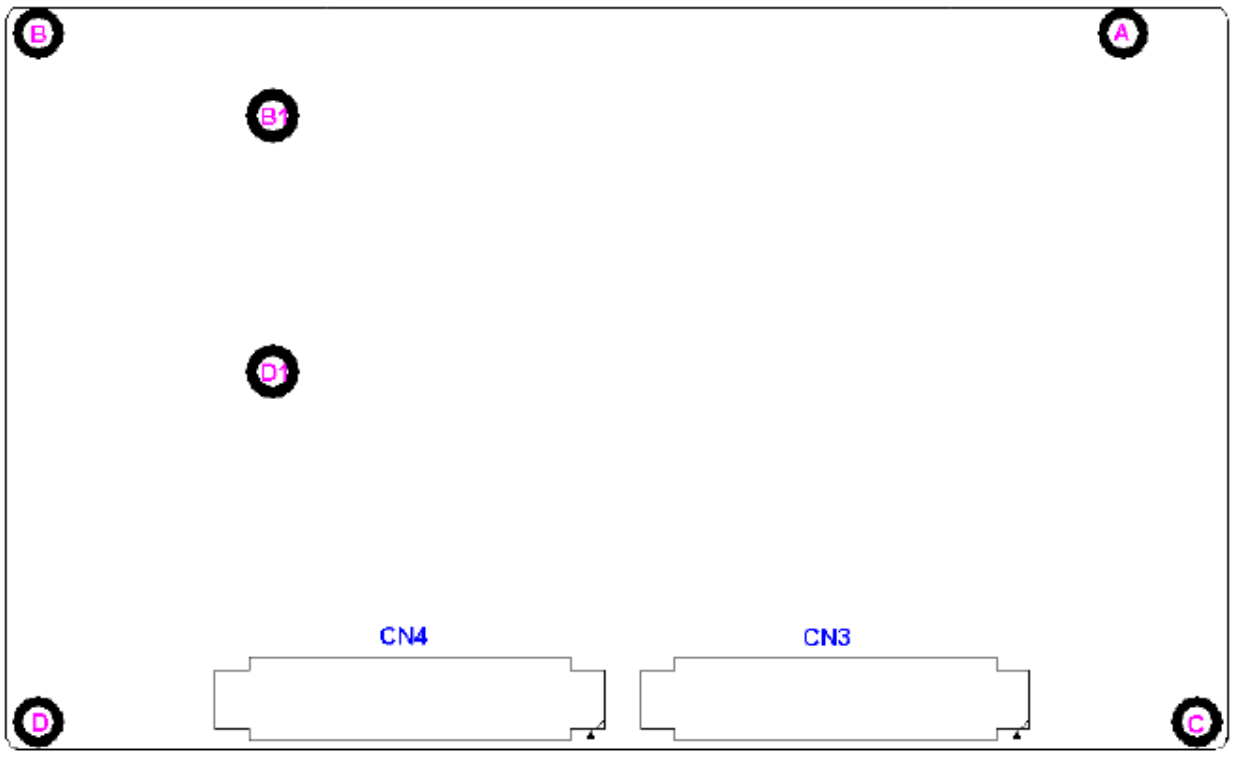
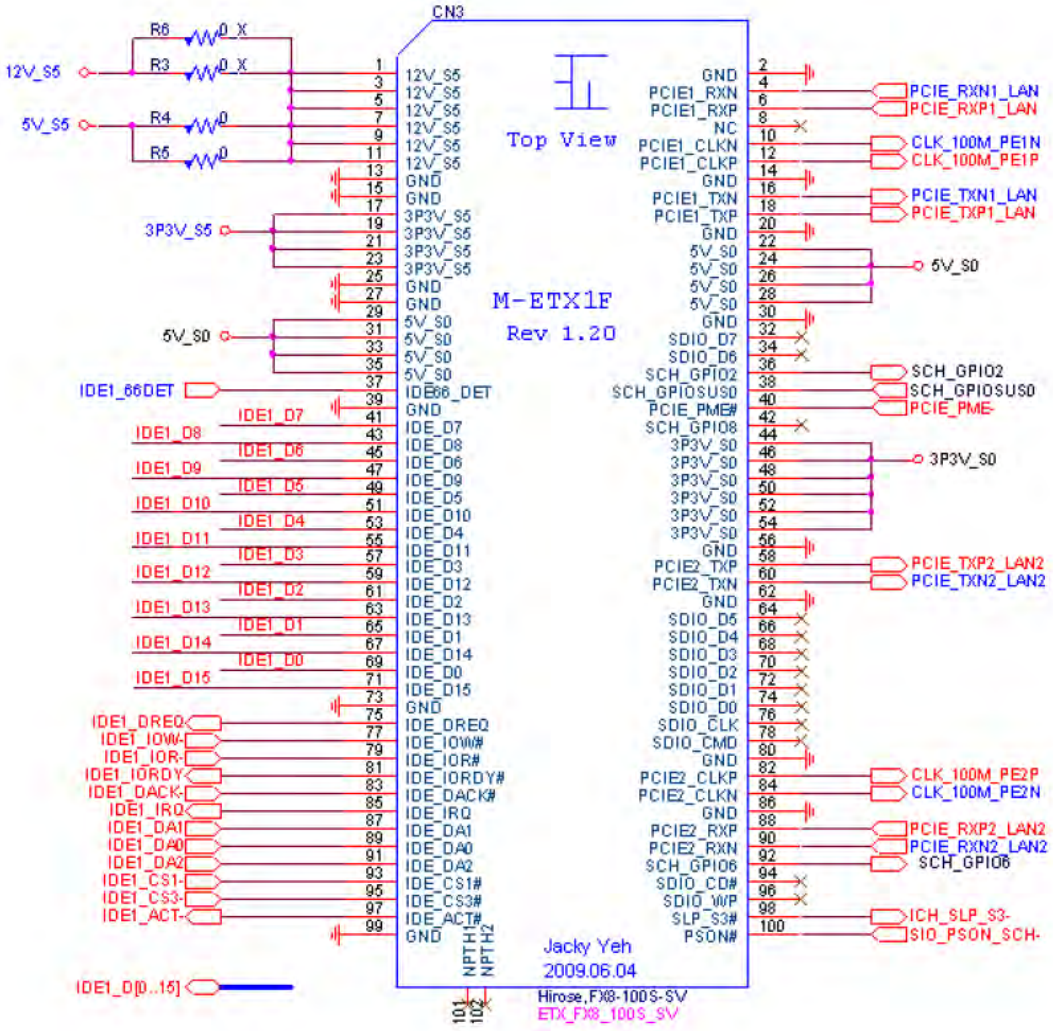


Figure 1.6: PB-703 R1.10 Board overview

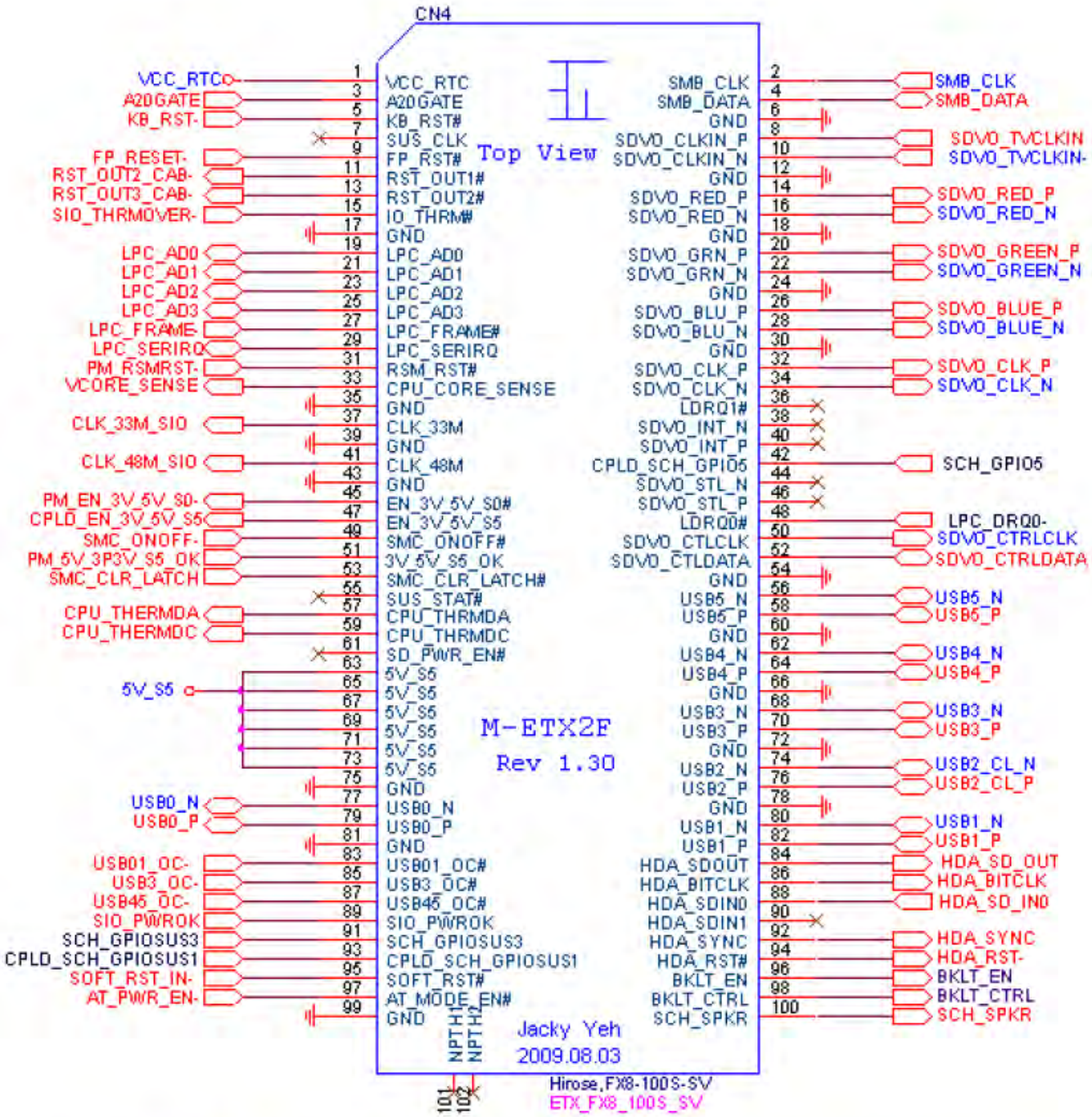
2.2.16 CN3

CN3 and CN4 are using HIROSE brand FX8C-100S-SV(21) type connectors ready for ASB-S700 CPU SOM module signaling and power supply as pins defined as follow：



Note 8：CN3 pins defined of PB-703 could be mapping from CN1 of ASB-S700 above.

2.2.17 CN4



Note 9：CN4 pins defined of PB-703 could be mapping from CN2 of ASB-S700 above.

2.2.18 PB-703 assembly

PCB dimension：115mm × 70mm ×1.6mm

Main assembly holes like A，B，C，D of PB-703 may adapt to A、B、C、Dholes of ASB-S700 (SOM) and

baseboard (PB-703) could be fixed by 4x 6mm +/- 0.1mm height nuts

Mini-PCI express card could be fixed by A1，B1，C1，D1：default A1，B1 for full-size mPCIe add-on card

and C1，D1 for half-size mPCIe add-on card.

Chapter 3 BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors. Non-fatal error messages usually appear on the screen along with the following instructions:

Press <F1> to RESUME

Write down the message and press the F1 key to continue the boot up sequence.

System configuration verification

These routines check the current system configuration against the values stored in the CMOS memory. If they do not match, the program outputs an error message. You will then need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The CMOS memory has lost power and the configuration information has been erased.

3.2 Award BIOS Setup

Awards BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del> immediately. This will allow you to enter Setup.

Standard CMOS Features

Use this menu for basic system configuration. (Date, time, IDE, etc.)

Advanced BIOS Features

Use this menu to set the advanced features available on your system.

Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system performance.

Integrated Peripherals

Use this menu to specify your settings for integrated peripherals. (Primary slave, secondary slave, keyboard, mouse etc.)

Power Management Setup

Use this menu to specify your settings for power management. (HDD power down, power on by ring, KB wake up, etc.)

PnP/PCI Configurations

This entry appears if your system supports PnP/PCI.

PC Health Status

This menu allows you to set the shutdown temperature for your system.

Frequency/Voltage Control

Use this menu to specify your settings for auto detect DIMM/PCI clock and spread spectrum.

Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While AWARD has designated the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

Set Supervisor/User Password

Use this menu to set Supervisor/User Passwords.

Save and Exit Setup

Save CMOS value changes to CMOS and exit setup.

Exit Without Saving

Abandon all CMOS value changes and exit setup.

Chapter 4 Installation of Drivers

This chapter describes the installation procedures for software and drivers under the windows XP. The software and drivers are included with the motherboard. The contents include Intel **chipset driver, VGA driver, LAN driver, Audio driver**

Installation instructions are given below.

> **Important Note:**
> After installing your Windows operating system (Windows 98SE/ME/2000/XP), you must install first the Intel Chipset Software Installation Utility before proceeding with the installation of drivers.

4.1 Intel Chipset Software Installation

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation Under Windows XP

1. Insert the Aplex product CD that comes with the board.
2. Click " **Intel® Chipset software installation Utility** "

3. When the Welcome screen appears, please click " Next " to Continue.

4. Click Yes to accept the software license agreement and proceed with the installation process.

5. On Readme Information screen, click Next to continue the installation.

6. The Setup process is now complete. Click Finish to restart the computer and for changes to take effect.

Intel® Chipset Device Software
Intel® Chipset Device Software
Setup Is Complete
intel
You must restart this computer for the changes to take effect. Would you like to restart the computer now?
Yes, I want to restart this computer now.
No, I will restart this computer later.
Click Finish, then remove any installation media from the drives.
Finish
Intel® Installation Framework

4.2 VGA Driver installation

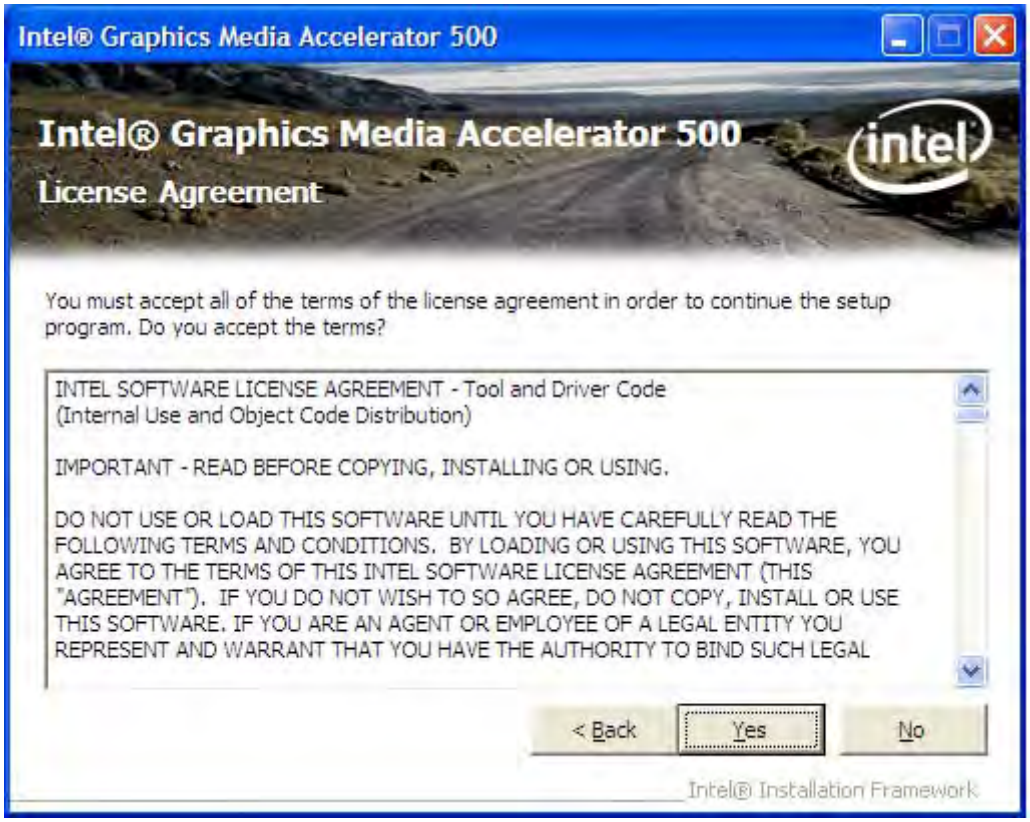
To install the VGA Driver follow the steps below to proceed with the installation.

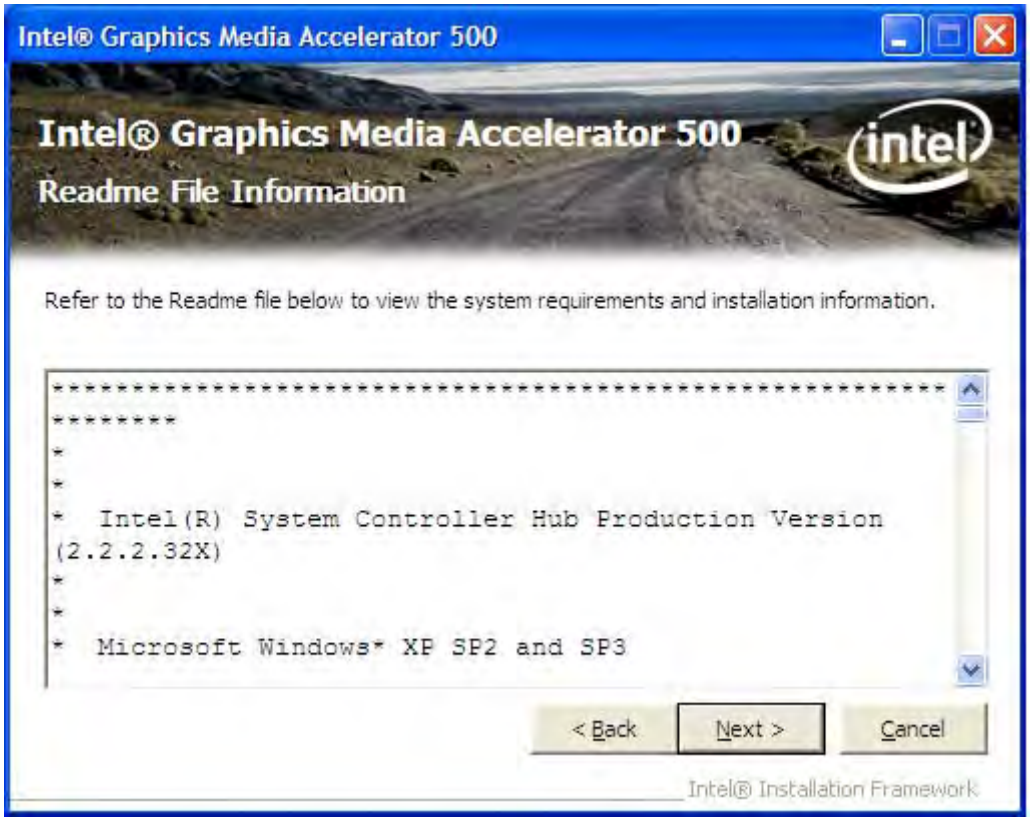
Step 1. Insert the Aplex product CD That comes with the board.

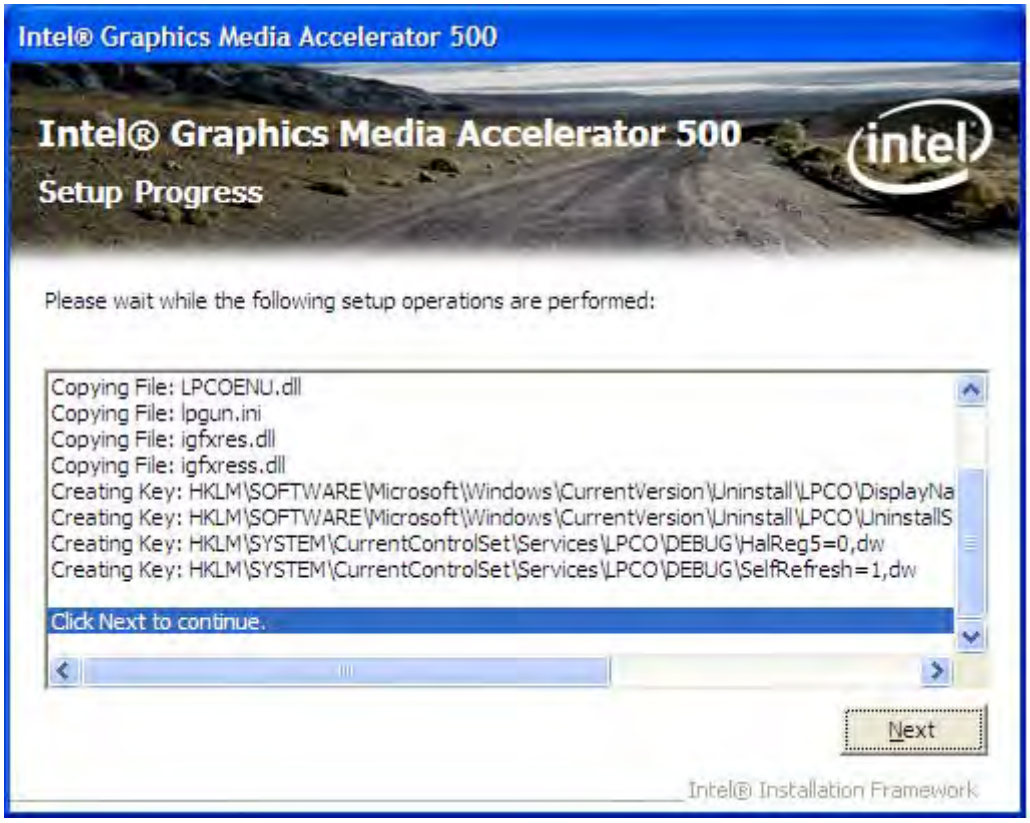
Step 2. Click " **Intel® VGA Chipset** "

Step 3. When the Welcome screen appears , click "**Next**" to continue.

Step 4. Click **YES** to agree with the license agreement and continue the installation.







Step 5. The Setup process is now complete. Click Finish to restart the computer as promoted and for changes to take effect. When the computer has restarted, the system will be able to find some devices. Restart your computer when prompted.

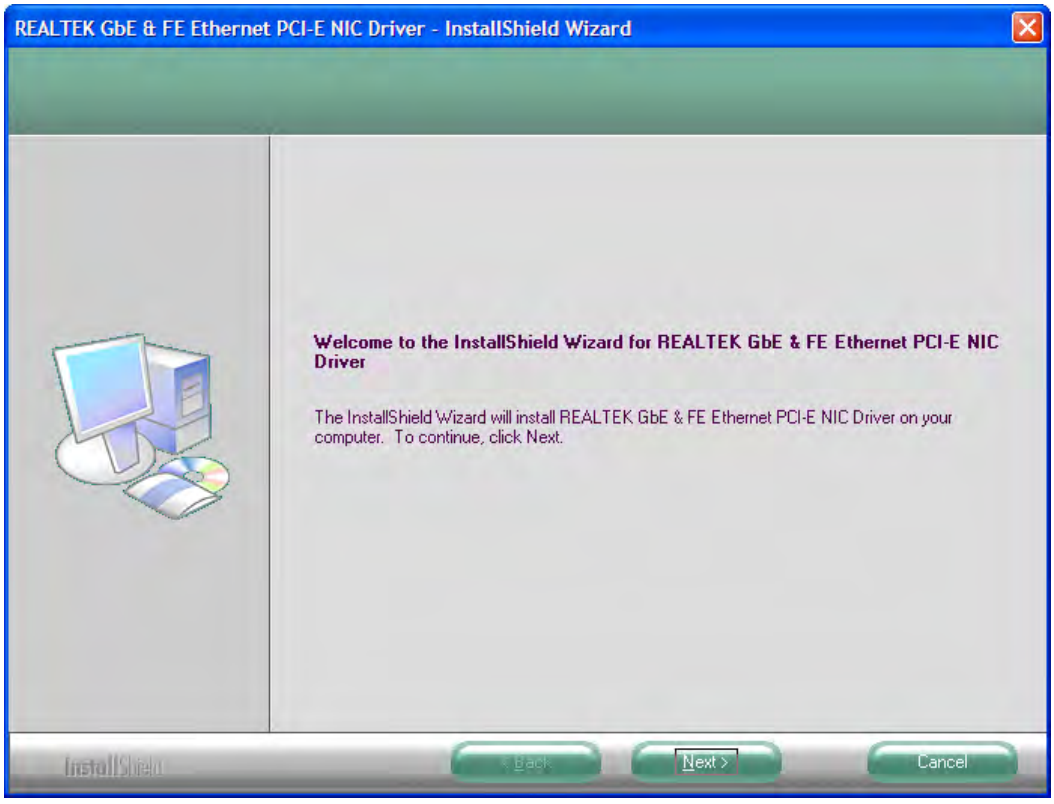
4.3 Intel PRO LAN Drivers installation

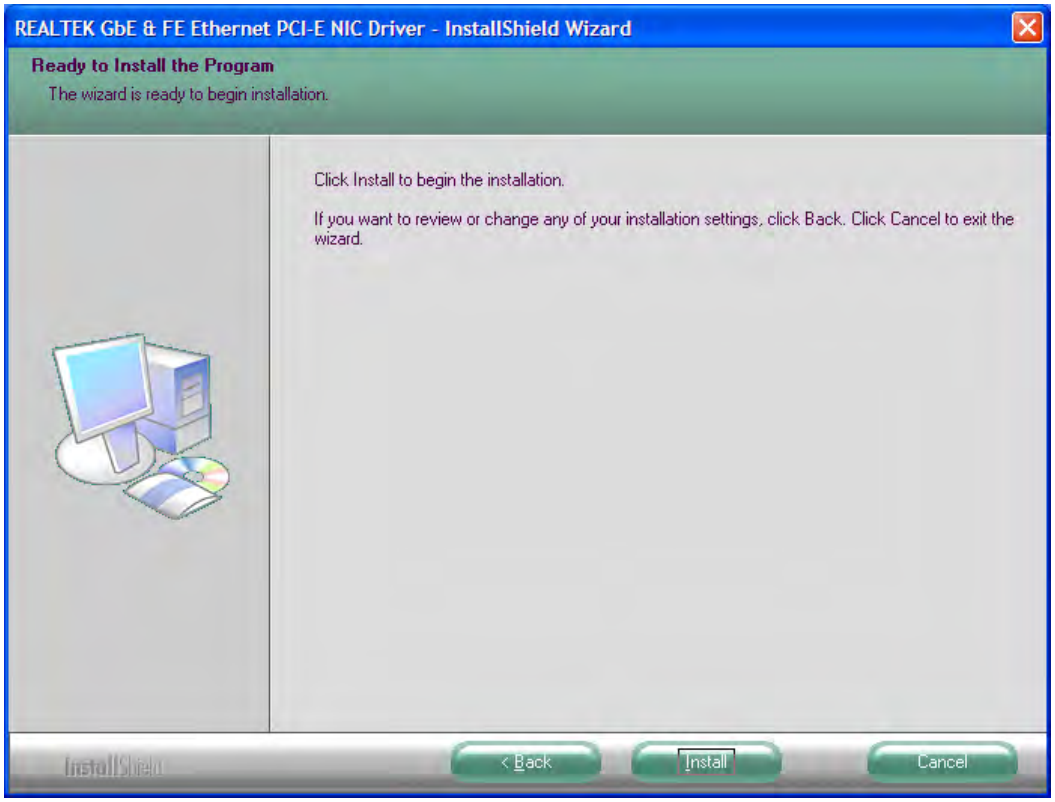
Follow the steps below to complete the installation of the Intel PRO LAN drivers.

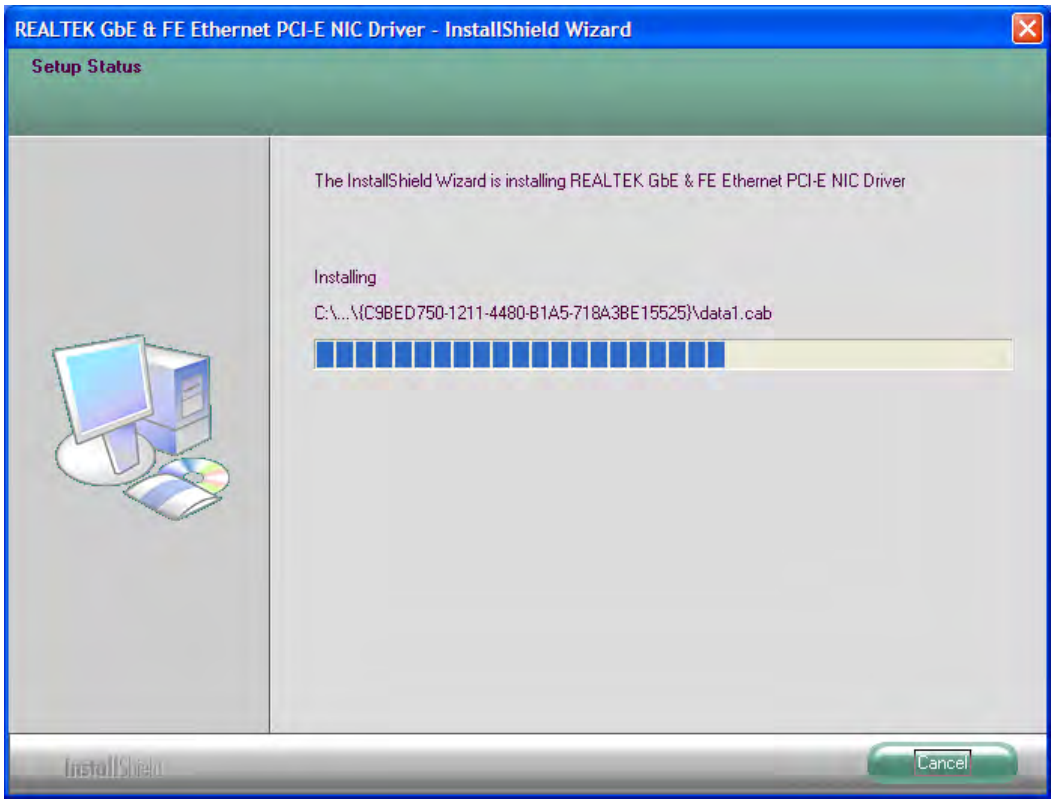
Step 1. Insert the Aplex product CD That comes with the board.

Step 2. Click “**Intel® Ethernet Driver**“

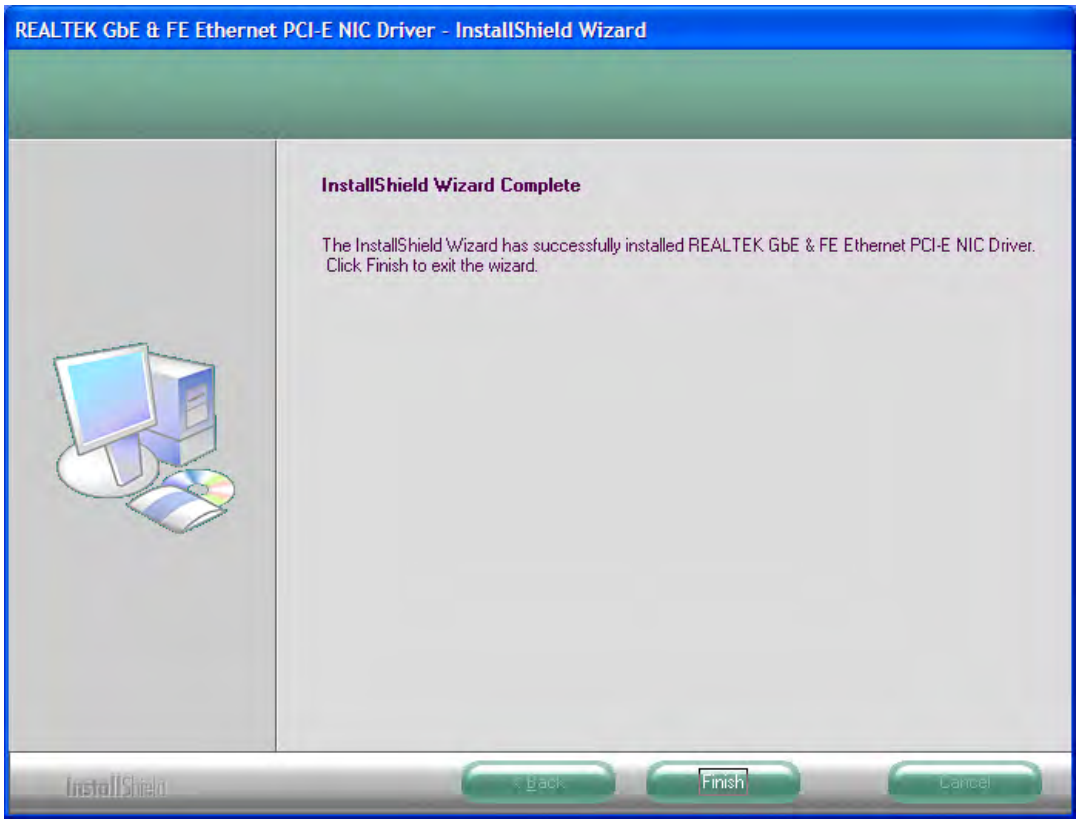
Step 3. When the Welcome screen appears , click “**Next**” to continue.




REALTEK GbE & FE Ethernet PCI-E NIC Driver - InstallShield Wizard
Ready to Install the Program
The wizard is ready to begin installation.
Click Install to begin the installation.
If you want to review or change any of your installation settings, click Back. Click Cancel to exit the wizard.
InstallShield
< Back
Install
Cancel


REALTEK GbE & FE Ethernet PCI-E NIC Driver - InstallShield Wizard
Setup Status
The InstallShield Wizard is installing REALTEK GbE & FE Ethernet PCI-E NIC Driver
Installing
C:\...\{C9BED750-1211-4480-B1A5-718A3BE15525}\data1.cab
InstallShield
Cancel

Step 4. Click “**Finish”** to restart the computer and for changes to take effect



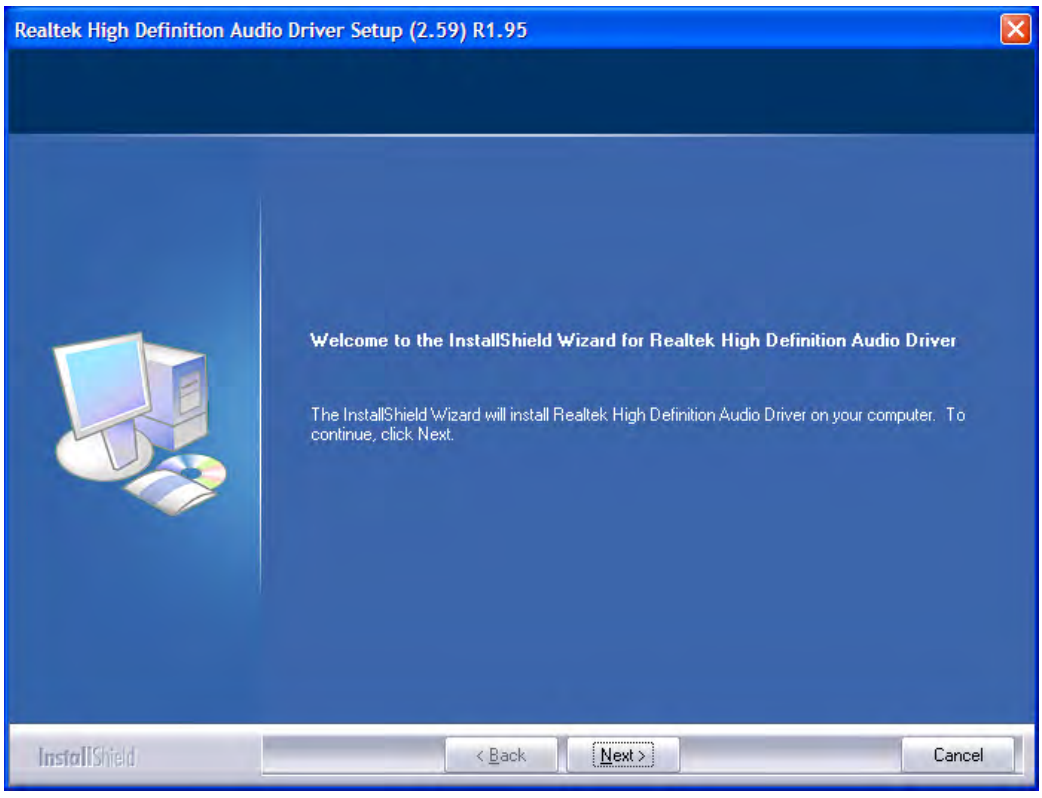
4.4 Realtek Audio Driver installation

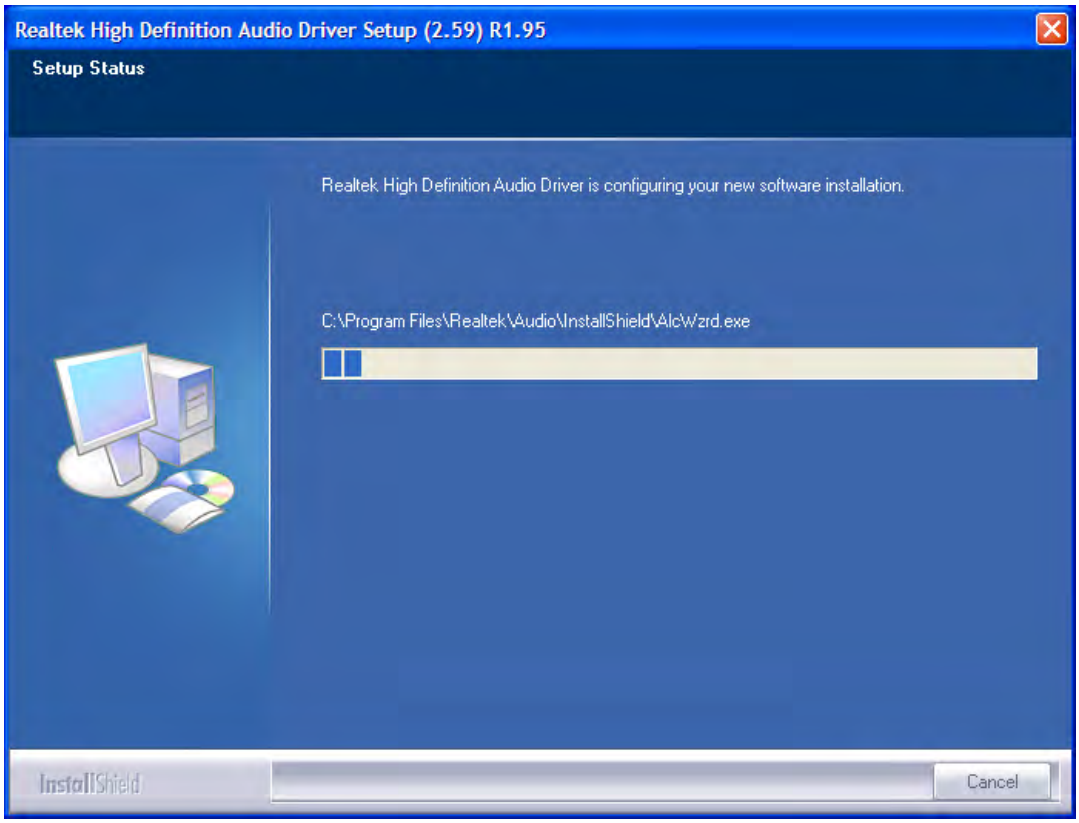
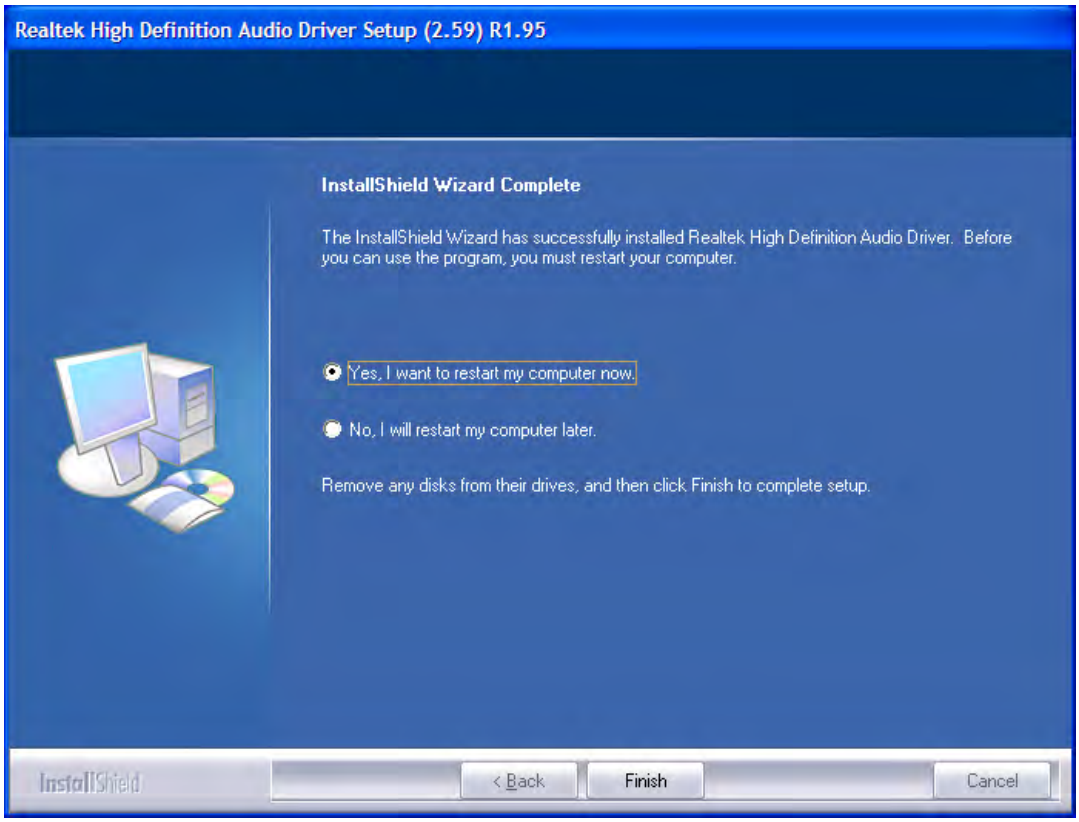
To install the Realtek codec Driver follow the steps below to proceed with the installation.

Step 1. Insert the Aplex product CD That comes with the board.

Step 2. Click “**Realtek ‘ Codec Sound system** “

Step 3. When the Welcome screen appears, click “**Next**” to continue.





Step 4. Click "**Finish"** to restart the computer and for changes to take effect.