



Datasound Labs. Ltd.

GX533 ETX Module

User Manual

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EMC

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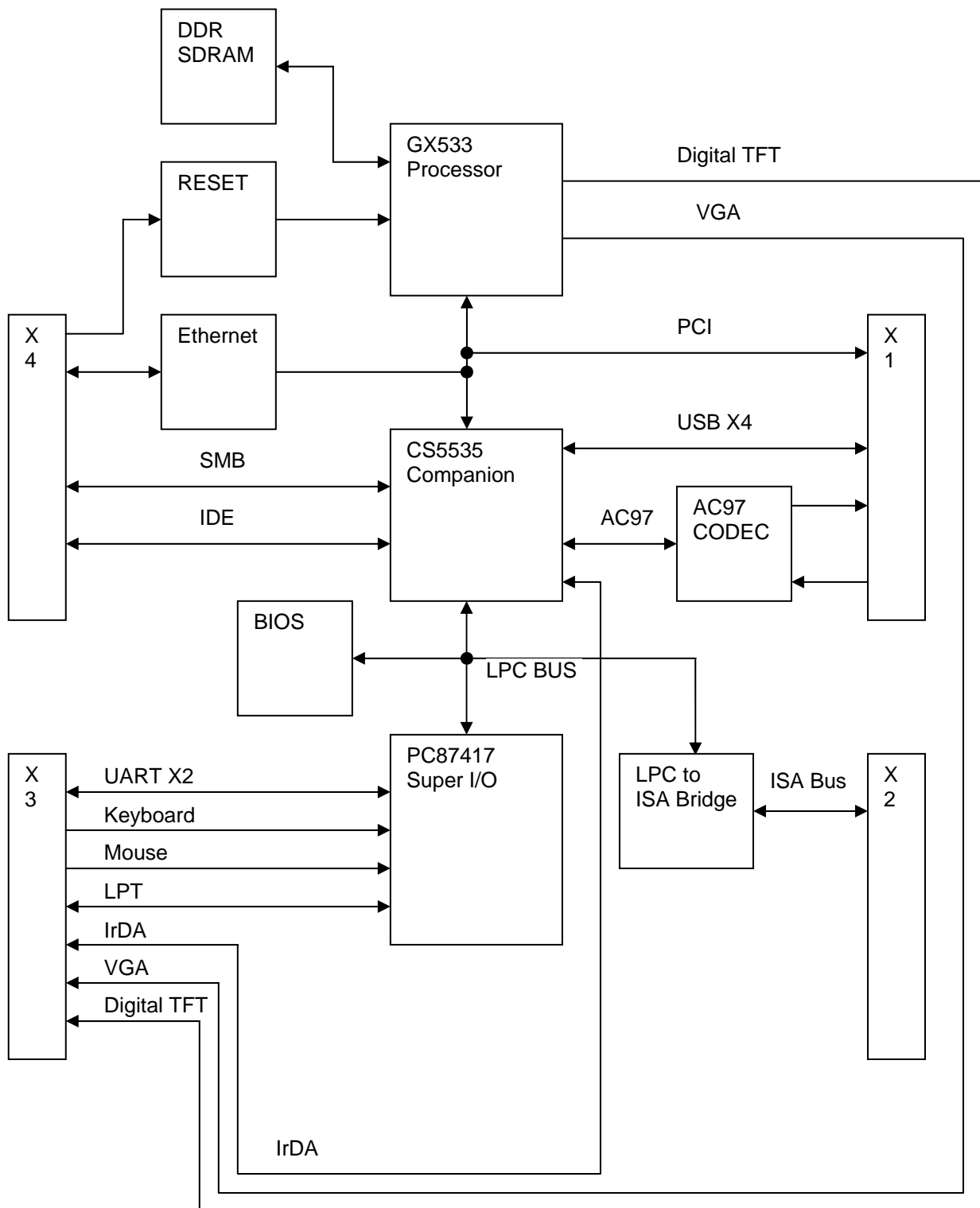
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1 Block Diagram.



2 Processor.

The AMD Geode™ GX533@1.1W processor core is a proven 32-bit x86 design that offers competitive performance with extremely low power consumption.

General Features:

- The processor runs at 400MHz, and gives a benchmark performance equivalent a Via 533 Centaur processor. Contact DSL for more information regarding AMD processor benchmarking.
- Power consumption of the processor is 1.1W @400Mhz; measured by running typical Microsoft® Windows® applications in a typical display mode with a background of vertical stripes (4-pixel wide) alternating between black and white with power management disabled.
- Graphics processor and Display controller, providing a display resolution up to 1600x1200x24 BPP. Jumper J2 selects compatibility (18bit) or enhanced mode (24bit) TFT signalling. See the description of X3 (9.3.1) for more information.
- Uses a Unified Memory Controller (UMC), where video memory resides in main memory. The BIOS is set to allocate 8MB of video memory.
- Supports both AMD 3DNow!™ and Intel MMX® instruction set extensions for the acceleration of multimedia applications.

The processor includes an integrated SDRAM controller, capable of interfacing to Double Data Rate (DDR) devices. This is interfaced to a single SODIMM connector, allowing SODIMM memory modules up to 512Mb in size to be used. The memory interface runs at 111MHz (222MHz DDR).

3 CS5535 I/O companion.

This device is designed to work in conjunction with the GX-series processors, and includes the following:

- GeodeLink™ PCI Bridge (South Bridge).
- Two 8259A equivalent interrupt controllers.
- 8254-equivalent timer.
- Two 8237-equivalent DMA controllers.
- Eight Multi-Function General Purpose Timers (MFGPTs).
- 32 GPIOs.
- Real Time Clock, with external battery backup.
- One System Management Bus (SMB) Controller.
- One ATA-5 compliant (UDMA/66), 3V signalling, IDE controller. The IDE interface supports one channel, which in turn supports two devices that can operate in PIO modes 1 to 4, MDMA modes 0 or 2, or UDMA/66 modes 0 to 4.

Note:-

The IDE interface of the CS5535 is not 5V tolerant. If an IDE device's interface signals at 5V, voltage level reducing devices are needed on the motherboard to prevent over-voltage.

- Audio Codec 97 (AC97) Controller.
- Two independent OpenHost Controller Interface (OHCI) v1.0 compliant Universal Serial Bus (USB) Controllers. Each controller provides two ports adhering to the USB v1.1 specification.
- Power Management Controller, supporting Legacy Power Management (PM), Advanced Power Management (APM) and Advanced Configuration and Power Interface (ACPI).
- A Low Pin Count (LPC) Port.

4 PC87374 Super I/O.

This device connects to the LPC bus and provides the following features:-

- ACCESS.bus™ Interface. This will be used to implement the I²C bus for ETX.
- IEEE 1284 compliant Parallel port.
- DS1287, MC146818 and PC87911 compatible RTC. This is not used as this functionality is provided by the I/O companion.
- PS/2 Keyboard and mouse controller.
- Two serial ports:-

The two TTL serial ports COM1 and COM2. They use the 'standard' IRQ and addresses for these ports.

The IrDA port, implemented on the ETX connectors, will be COM3. It will use the 'standard' IRQ and address for this port.

PORT	IRQ	ADDRESS
COM1	4	0x3F8
COM2	3	0x2F8
COM3	4	0x3E8

The floppy disk interface is not implemented on the ETX module.

5 W8362 LPC to ISA Bridge

This device connects to the LPC bus and provides the following ISA bus features:-

- LDRQ# (LPC DMA) & SERIRQ (serial IRQ)
- Full ISA Bus Support (except ISA Bus Mastering, 16 bit I/O and 16bit Memory R/W)
- 5V compliant ISA interface
- IRQ Serializer for ISA Parallel IRQ transfer to Serial IRQ
- Supports 3 fully ISA Compatible Slots without Buffering

6 Power Supply and regulators.

Power will be supplied via the ETX connector.

There is no on board regulation for the 5V supply. The external power supply must be regulated and provide an output of 5V \pm 5%, according to the ETX specification.

Three switch-mode regulators will provide the +3.3V for the main on-board logic; processor core voltage of 1.5V; and 2.5V for the memory module.

These will be all generated from the 5V that is supplied through the ETX connector.

In addition there will be two linear regulators providing standby voltages for 3.3V and 1.5V from the 5V standby voltage supplied through the ETX connector.

7 Ethernet.

The 10/100 base T Ethernet controller is a National Semiconductor DP83815, IEEE 802.3 compliant MacPHYTER™ chip. This interfaces directly onto the PCI bus.

Signals for Link, Speed and Activity LED's are provided.

As per the ETX specification the Ethernet magnetics need to be implemented on the motherboard.

8 ETX Connectors.

X1

- The PCI Bus is fully implemented to this connector, allowing for three PCI devices to be connected externally. The on board Ethernet effectively uses one PCI slot.
- All four USB connection sets are implemented. Protection, current limiting and fusing components should be fitted to the ETX baseboard.
- Two pairs of line level audio outputs, and a single microphone input are connected. Any amplification etc. should be performed on the ETX baseboard.

X2

- The Industry Standard Architecture (ISA) bus is implemented to this connector.

X3

- VGA Analog signals, including DDC signals. Protection should be supplied on the ETX baseboard.
- Digital Flat Panel signals are connected. A sub set of the Geode™ 24-bit output will be used to provide the 18-bit signals required in the ETX specification.
- LVDS outputs are not supported.
- Both JILI and JIDI signals are not supported.
- Television outputs are not supported.
- Two, fully functional, serial port outputs are implemented. The signals are TTL level, RS232 level translation should be done on the ETX baseboard.
- PS/2 Keyboard and Mouse signals are connected. Protection should be supplied on the ETX baseboard.
- Parallel port signals are connected, A Floppy disk interface is not supported.
- IrDA are connected. The Infrared transceiver should be implemented on the ETX baseboard.

X4

- Primary IDE signals are implemented.
- Secondary IDE is not supported.
- Ethernet signals are connected. Protection and magnetics should be supplied on the ETX baseboard.
- System speaker connections are provided.
- Battery connections to protect RTC data, are provided.
- I²C connections are provided.
- SM Bus connections are provided.
- ATX power supply control signals have been provided. The power good signal is not required by the ETX module. This signal can be used as an active low reset signal
- USB over current signal connection is provided.
- The keyboard inhibit signal is not connected.

Deviations

- For 24-bit TFT operation the module will, optionally, use the JILI, JIDI and TV output connections to pass the six least significant bits to the motherboard. Jumper J2 will control these signals. When J2 is in the 1-2 position (pin 1 is indicated by the square pad) the module is in compatibility mode whereby the additional 6 bits are tri-stated. When the jumper is in the 2-3 position the 24-bit mode is implemented. See Section 9.3.1
- Secondary IDE is not implemented.
- Floppy Disk interface is not implemented.

9 ETX Signals

GND

Ground. All 41 GND pins on the ETX module should be connected to the baseboard ground plane.

VCC

+5V $\pm 5\%$ power supply. All 21 VCC pins on the ETX module should be connected to the baseboard +5V plane.

3V

+3.3V $\pm 5\%$ supply voltage generated onboard the ETX module. These two pins may be used as a power supply for external devices. Maximum allowed external load is 500mA.

Do not connect 3.3V pins to an external 3.3V supply.

RESERVED

These pins are reserved for future use or for manufacturing and test purposes. Do not connect external signals to these pins.

9.1 Connector X1

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ3#	10	GNT3#
11	GNT2#	12	3V
13	REQ2#	14	GNT1#
15	REQ1#	16	3V
17	GNT0#	18	RESERVED
19	VCC	20	VCC
21	SERIRQ	22	REQ0#
23	AD0	24	3V
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	CBE0#	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	AUXAL
39	AD11	40	MIC
41	AD12	42	AUXAR
43	AD13	44	ASVCC
45	AD14	46	SNDL
47	AD15	48	ASGND
49	CBE1#	50	SNDR

Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	PAR	54	SERR#
55	GPERR#	56	RESERVED
57	PME#	58	USB2#
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB3#
63	IRDY#	64	STOP#
65	FRAME#	66	USB2
67	GND	68	GND
69	AD16	70	CBE2#
71	AD17	72	USB3
73	AD19	74	AD18
75	AD20	76	USB0#
77	AD22	78	AD21
79	AD23	80	USB1#
81	AD24	82	CBE3#
83	VCC	84	VCC
85	AD25	86	AD26
87	AD28	88	USB0
89	AD27	90	AD29
91	AD30	92	USB1
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

9.1.1 PCI Signals - General

All signals are 3.3V level PCI signals. All PCI signal pull-ups are integrated on the ETX board. Pullups may be to either a 3.3V or 5V supply, as detailed in the PCI specification. Any external PCI devices that have "5V tolerance" pins should have these pins connected to an appropriate 5V reference voltage as per the manufacturer's recommendation. This module will not, therefore, have 3.3V to 5V translation on-board. If a 5V PCI slot is required on a motherboard, translation will be required.

If translation is not supplied on any motherboard incorporating a 5V PCI component the processor on this ETX module will be damaged!

PCICLK1..4

PCI clock outputs for up to 4 external PCI slots or devices.

These clocks should be routed for 700pS total delay between the ETX connector pin and the pin of the PCI clock device.

REQ[0..3]#

Bus Request signals for up to 4 external bus mastering PCI devices. When asserted, a PCI device is requesting PCI bus ownership from the arbiter. This module supports 3 REQ/GNT pairs (0 to 2 inclusive).

GNT[0..3]#

Grant signals to PCI Masters. When asserted by the arbiter, the PCI master has been granted ownership of the PCI bus.

AD[0..31]

PCI Address and Data Bus Lines. These lines carry the address and data information for PCI transactions.

CBE[0..3]#

PCI Bus Command and Byte Enables. Bus command and byte enables are multiplexed in these lines for address and data phases, respectively.

PAR

Parity bit for the PCI bus. Generated as even parity across AD[31:0] and CBE[3:0]#.

SERR#

System Error. Not Implemented. Signal on ETX is pulled up.

GPERR#

Parity Error. Not Implemented. Signal on ETX is pulled up.

PME#

Power management event.

LOCK#

Lock Resource Signal. Not Implemented. Signal on ETX is pulled up.

DEVSEL#

Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.

TRDY#

Target Ready. This pin indicates that the target is ready to complete the current data phase of a transaction.

IRDY#

Initiator Ready. This signal indicates that the initiator is ready to complete the current data phase of a transaction.

STOP#

Stop. This signal indicates that the target is requesting that the master stop the current transaction.

FRAME#

Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. The access will be either an output driven by the Northbridge on behalf of the CPU, or an input during PCI master access.

PCIRST#

PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal is asserted during system reset.

INTA#, INTB#, INTC#, INTD#

PCI interrupts. These interrupts are sharable and are typically wired in rotation to PCI slots or devices.

IDSEL

This pin is not present on the ETX module connector, but it is present on each PCI slot connector or device. IDSEL is an input to the device that is used to set the device's configuration address for PCI configuration cycles. The IDSEL pin of each device is typically connected to one of the AD lines in order to set a unique configuration address. In ETX systems, the four external bus slots or devices are assumed to use AD[19..22] for IDSEL connections.

AD24 is used on-board for the Ethernet.

AD28 is used on-board for the 5535 South-bridge.

AD29 is used on-board for the 5535 USB controller.

9.1.2 USB Signals

USB signal termination components are integrated on the ETX board. In applications using external USB devices, additional USB protection components must be included on the baseboard, USB data signals should be routed as differential pairs.

For information regarding over-current detection on the USB, refer to signal OVCR#

USB0, USB0#

Universal Serial Bus Port 0. These are the serial data pairs for USB Port 0. USB0 – positive signal. USB0# – negative signal.

USB1, USB1#

Universal Serial Bus Port 1. These are the serial data pairs for USB Port 1. USB1 – positive signal. USB1# – negative signal.

USB2, USB2#

Universal Serial Bus Port 2. These are the serial data pairs for USB Port 2. USB2 – positive signal. USB2# – negative signal.

USB3, USB3#

Universal Serial Bus Port 3. These are the serial data pairs for USB Port 3. USB3 – positive signal. USB3# – negative signal.

9.1.3 Audio Signals

SNDL/ SNDR

Line-level stereo output left/ right. These outputs have a nominal level of 1 volt RMS into a 10K impedance load. These outputs cannot drive low-impedance speakers directly.

AUXAL/ AUXAR

Auxiliary A input left/ right. Normally intended for connection to an internal or external CD-ROM analog output or a similar line-level audio source. Minimum input impedance is 5KOhm. Nominal input level is 1 volt RMS.

MIC

Microphone input. Minimum input impedance is 5KOhm, max. input voltage is 0.15 **Vp-p**.

ASGND

Analog ground for sound controller. Use this signal ground for an external amplifier in order to achieve lowest audio noise levels.

ASVCC

Analog supply voltage for sound controller. This is an output which is used for production test only. Do not make external connections to this pin.

9.1.4 Miscellaneous

SERIRQ

Serial interrupt request. This pin is used to support the serial interrupt protocol.

9.2 Connector X2

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SD14	4	SD15
5	SD13	6	MASTER#
7	SD12	8	DREQ7
9	SD11	10	DACK7#
11	SD10	12	DREQ6
13	SD9	14	DACK6#
15	SD8	16	DREQ5
17	MEMW#	18	DACK5#
19	MEMR#	20	DREQ0
21	LA17	22	DACK0#
23	LA18	24	IRQ14
25	LA19	26	IRQ15
27	LA20	28	IRQ12
29	LA21	30	IRQ11
31	LA22	32	IRQ10
33	LA23	34	IO16#
35	GND	36	GND
37	SBHE#	38	M16#
39	SA0	40	OSC
41	SA1	42	BALE
43	SA2	44	TC
45	SA3	46	DACK2#
47	SA4	48	IRQ3
49	SA5	50	IRQ4

Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	SA6	54	IRQ5
55	SA7	56	IRQ6
57	SA8	58	IRQ7
59	SA9	60	SYSCLK
61	SA10	62	REFSH#
63	SA11	64	DREQ1
65	SA12	66	DACK1#
67	GND	68	GND
69	SA13	70	DREQ3
71	SA14	72	DACK3#
73	SA15	74	IOR#
75	SA16	76	IOW#
77	SA18	78	SA17
79	SA19	80	SMEMR#
81	IOCHRDY	82	AEN
83	VCC	84	VCC
85	SD0	86	SMEMW#
87	SD2	88	SD1
89	SD3	90	NOWS#
91	DREQ2	92	SD4
93	SD5	94	IRQ9
95	SD6	96	SD7
97	IOCHK#	98	RSTDRV
99	GND	100	GND

9.2.1 ISA Signals

All required signal pull-ups are integrated into the ETX module. In some applications it may be desirable to add additional signal termination components to the baseboard.

SD[0..15]

These signals provide data bus bits 0 to 15 for any peripheral devices. All 8-bit devices use SD0[0..7] for data transfers. 16-bit devices use SD[0..15].

To support 8-bit devices, the data on SD[8..15] is gated to SD[0..7] during 8-bit transfers to these devices. 16-bit CPU cycles will be automatically converted into two 8-bit cycles for 8-bit peripherals.

SA[0..19]

Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA[17..23] allow access of up to 16MB of memory. SA[0..19] are gated on the ISA-bus when BALE is high and latched on to the falling edge of BALE.

SBHE#

Bus High Enable indicates a data transfer on the upper byte of the data bus SD[8..15]. 16-bit I/O devices use SBHE# to enable data bus buffers on SD[8..15].

BALE

BALE is an active-high pulse generated at the beginning of any bus cycle initiated by a CPU module. It indicates when the SA[0..19], LA17.23, AEN, and SBHE# signals are valid.

AEN

AEN is an active-high output that indicates a DMA transfer cycle. Only resources with a active DACK# signal should respond to the command lines when AEN is high.

MEMR#

MEMR# instructs memory devices to drive data onto the data bus. MEMR# is active for all memory read cycles.

SMEMR#

SMEMR# instructs memory devices to drive data onto the data bus. SMEMR# is active for memory read cycles to addresses below 1MB.

MEMW#

MEMW# instructs memory devices to store the data present on the data bus. MEMW# is active for all memory write cycles.

SMEMW#

SMEMW# instructs memory devices to store the data present on the data bus. SMEMW# is active for all memory write cycles to address below 1MB.

IOR#

I/O read instructs an I/O device to drive its data onto the data bus. It may be driven by the CPU or by the DMA controller. IOR# is inactive (high) during refresh cycles.

IOW#

I/O write instructs an I/O device to store the data present on the data bus. It may be driven by the CPU or by the DMA controller. IOW# is inactive (high) during refresh cycles.

IOCHK#

IOCHK# is an active-low input signal that indicates that an error has occurred on the module bus. If I/O checking is enabled on the CPU module, an IOCHK# assertion by a peripheral device sends a NMI to the processor.

IOCHRDY

The I/O Channel Ready is pulled low in order to extend the read or write cycles of any bus access when required. The CPU, DMA controllers or refresh controller can initiate the cycle. Any peripheral that cannot present read data or strobe in write data within this amount of time use IOCHRDY to extend these cycles.

This signal should not be held low for more than 2.5 μ s for normal operation. Any extension to more than 2.5 μ s does not guarantee proper DRAM memory content due to the fact that memory refresh is disabled while IOCHRDY is low.

M16#

The Winbond LPC to ISA bridge does not support 16 bit I/O access.

IO16#

The Winbond LPC to ISA bridge does not support 16 bit memory access.

REFSH#

REFSH# is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 μ s in order to prevent loss of DRAM data.

NOWS#

The Zero wait state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default the CPU inserts 4 wait states for 8-bit transfers and 1 wait state for 16-bit transfers.

MASTER#

The Winbond LPC to ISA bridge does not support bus mastering.

SYSCLK

SYSCLK has a nominal frequency of 8 MHz with a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.

OSC

OSC has a nominal frequency of 14.31818 MHz with a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.

RESETDRV

This active-high output is system reset generated from CPU module. It is responsible for resetting external devices.

DREQ[0, 1, 2, 3, 5, 6, 7]

The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU modules DAM controllers. DREQ0..3 are used for transfers between 8-bit I/O adapters and system memory. DREQ5..7 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on the CPU modules.

DACK[0, 1, 2, 3, 5, 6, 7]#

DMA acknowledge 0..3 and 5.7 are used to acknowledge DMA requests. They are active-low.

TC

The active-high output TC indicates that one of the DMA channels has transferred all data.

IRQ[3..7, 9,15]

These are the asynchronous interrupt request lines. IRQ0, 1, 2 and 8 are not available as external interrupts because they are used internally on the CPU module. All IRQ signals are active-high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest

priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt service routine).

9.3 Connector X3

9.3.1 DIGITAL FLAT PANEL INTERFACE

The ETX digital flat panel interface, normally, supports 18-bit panels.

The processor in this design is capable of driving 24-bit digital flat panels.

An on-board jumper (J2) allows the selection of 'compatibility mode', whereby all signals meet the ETX specification, or 24-bit mode, whereby a number of unused signals will carry the additional 6 data bits.

The functions of the shaded pins differ between the compatibility mode and the 24-bit mode.

The unshaded pins have identical functions regardless of the mode.

18 bit

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#	10	DDDA
11	B4	12	SHFCLK
13	B5	14	EN
15	GND	16	GND
17	B1	18	B3
19	B0	20	B2
21	GND	22	GND
23	G2	24	G5
25	G3	26	G4
27	GND	28	GND
29	R4	30	G1
31	R5	32	G0
33	GND	34	GND
35	R1	36	R3
37	R0	38	R2
39	VCC	40	VCC
41	JILI_DAT	42	VSYNC
43	JILI_CLK	44	BLON#
45	HSYNC	46	DIGON
47	COMP	48	Y
49	SYNC	50	C

24 bit

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#	10	DDDA
11	B6	12	SHFCLK
13	B7	14	EN
15	GND	16	GND
17	B3	18	B5
19	B2	20	B4
21	GND	22	GND
23	G4	24	G7
25	G5	26	G6
27	GND	28	GND
29	R6	30	G3
31	R7	32	G2
33	GND	34	GND
35	R3	36	R5
37	R2	38	R4
39	VCC	40	VCC
41	B1	42	VSYNC
43	B0	44	BLON#
45	HSYNC	46	DIGON
47	R1	48	G1
49	R0	50	G0

9.3.2 VGA Signals

External termination components are required on the VGA analog video outputs.

HSY

Horizontal Sync: This output supplies the horizontal synchronization pulse to the CRT monitor.

VSY

Vertical Sync: This output supplies the vertical synchronization pulse to the CRT monitor.

R, G, B

Red, green and blue analog video output signals for CRT monitors. These lines should be terminated with 75 ohms to ground at the video connector.

DDCK, DDDA

These two pins can be used for a DDC interface between the graphics controller chip and the CRT monitor.

9.3.3 Digital Flat Panel Interface Signals

R[0..7], G[0..7], B[0..7]

Parallel digital signals for red, green and blue pixel data.

HSYNC

Horizontal Sync: This output supplies the horizontal synchronization pulse for flat panels. This signal is named LP (Line Pulse) in some flat panel literature.

VSYNC

Vertical Sync: This output supplies the vertical synchronization pulse for flat panels. This signal is named FLM (First Line Marker) in some flat panel literature.

DE

Data enable signal. Usage depends on display type.

SHCLK

Panel data clock signal.

DIGON

Controls panel digital power.

BLON#

Controls backlight power..

JILI_CLK

Not Implemented. This line is tri-stated in compatibility mode and Blue bit 0 in 24 bit mode.

JILI_DAT

Not Implemented. This line is tri-stated in compatibility mode and Blue bit 1 in 24 bit mode.

DETECT#

Not Implemented.

4.3.4. Television Output Signals

SYNC

Not Implemented. This line is tri-stated in compatibility mode and Red bit 0 in 24 bit mode.

Y

Not Implemented. This line is tri-stated in compatibility mode and Green bit 1 in 24 bit mode.

C

Not Implemented. This line is tri-stated in compatibility mode and Green bit 0 in 24 bit mode.

COMP

Not Implemented. This line is tri-stated in compatibility mode and Red bit 1 in 24 bit mode.

9.3.4 Serial Port Signals

Note that all serial port signals on the ETX module connectors are logic level signals. External transceiver devices are necessary for the conversion of the logic level signals to the desired physical interface such as RS232, RS422, or RS485.

DTR1#, DTR2#

Active-low data terminal ready outputs for the serial port. Handshake output signal notifies the modem that the UART is ready to establish a data communication link.

RI1#, RI2#

Active-low input is for the serial port. Handshake signals notify the UART when a telephone ring signal is detected by the modem.

TXD1, TXD2

Transmitter serial data output from serial port.

RXD1, RXD2

Receiver serial data input.

CTS1#, CTS2#

Active-low input for serial ports. Handshake signals notify the UART when the modem is ready to receive data.

RTS1#, RTS2#

Active-low output for serial port. Handshake signals notify the modem when the UART is ready to transmit data.

DCD1#, DCD2#

Active-low input for serial port. Handshake signals notify the UART when a carrier signal is detected by the modem.

DSR1#, DSR2#

This active-low input is for serial port. Handshake signals are use to notify the UART that the modem is ready to establish the communication link.

9.3.5 PS/2 Keyboard, PS/2 Mouse Signals

KBDAT

Bi-directional keyboard data signal.

KBCLK

Keyboard clock signal.

MSDAT

Bi-directional mouse data signal.

MSCLK

Mouse clock signal.

4.3.7. IRDA (SIR) Signals

IRTX, IRRX

Infrared transmit and receive pins.

9.3.6 Parallel Port Signals

The parallel port signals require external termination components.

LPT/FLPY#

Not Implemented. – Only the parallel port is implimented

STB#

This active-low signal is used to strobe the printer data into the printer.

AFD#

This active-low output tells the printer to automatically feed the next single line after each preceding line has been printed.

PD[0..7]

This bi-directional parallel data bus is used to transfer information between the CPU and the peripherals.

ERR#

This active-low signal indicates an error situation has occurred at the printer.

INIT#

This active-low signal is used to initiate the printer when low.

SLIN#

This active-low signal selects the printer.

ACK#

This active-low output from the printer indicates that it has received the previous data and that it is ready to receive new data.

BUSY#

This signal indicates that the printer is busy and not ready to receive new data.

PE

This signal indicates that the printer is out of paper.

SLCT#

This active-high output from the printer indicates that its power is on.

9.4 Connector X4

Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	KBINH	10	LILED
11	RSMRST#	12	ACTLED
13	ROMKBCS#	14	SPEEDLED
15	EXT_PRG	16	I2CLK
17	VCC	18	VCC
19	OVCR#	20	GPCS#
21	EXTSMI#	22	I2DAT
23	SMBCLK	24	SMBDATA
25	SIDE_CS3#	26	SMBALRT#
27	SIDE_CS1#	28	DASP_S
29	SIDE_A2	30	PIDE_CS3#
31	SIDE_A0	32	PIDE_CS1#
33	GND	34	GND
35	PDIAG_S	36	PIDE_A2
37	SIDE_A1	38	PIDE_A0
39	SIDE_INTRQ	40	PIDE_A1
41	BATLOW#	42	GPE1#
43	SIDE_AK#	44	PIDE_INTRQ
45	SIDE_RDY	46	PIDE_AK#
47	SIDE_IOR#	48	PIDE_RDY
49	VCC	50	VCC

Pin	Signal	Pin	Signal
51	SIDE_IOW#	52	PIDE_IOR#
53	SIDE_DRQ	54	PIDE_IOW#
55	SIDE_D15	56	PIDE_DRQ
57	SIDE_D0	58	PIDE_D15
59	SIDE_D14	60	PIDE_D0
61	SIDE_D1	62	PIDE_D14
63	SIDE_D13	64	PIDE_D1
65	GND	66	GND
67	SIDE_D2	68	PIDE_D13
69	SIDE_D12	70	PIDE_D2
71	SIDE_D3	72	PIDE_D12
73	SIDE_D11	74	PIDE_D3
75	SIDE_D4	76	PIDE_D11
77	SIDE_D10	78	PIDE_D4
79	SIDE_D5	80	PIDE_D10
81	VCC	82	VCC
83	SIDE_D9	84	PIDE_D5
85	SIDE_D6	86	PIDE_D9
87	SIDE_D8	88	PIDE_D6
89	GPE2#	90	CBLID_P#
91	RXD#	92	PIDE_D8
93	RXD	94	SIDE_D7
95	TXD#	96	PIDE_D7
97	TXD	98	HDRST#
99	GND	100	GND

9.4.1 IDE Signals

Primary IDE is supported.

Secondary IDE channels are not implemented.

For each signal, the first signal name is for the primary channel and the second signal name is for the secondary channel.

PIDE_D0..15/ SIDE_D0..15

IDE Data Bus. .

PIDE_A[0..2]/ SIDE_A[0..2]

IDE Address Bus. .

PIDE_CS1#/ SIDE_CS1#

IDE Chip Select 1. This is the Chip Select 1 command output pin that enables the IDE device to watch the Read/Write Command.

PIDE_CS3#/ SIDE_CS3#

IDE Chip Select 3. This is the Chip Select 3 command output pin that enables the IDE device to watch the Read/Write Command.

PIDE_DRQ/ SIDE_DRQ

IDE DMA Request for IDE Master. This signal is asserted by an IDE device. It will be active-high in DMA or Ultra-33 mode and always be inactive-low in PIO mode.

PIDED_AK#/ SIDED_AK#

IDE DACK# for IDE Master. This signal grants the IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.

PIDE_RDY/ SIDE_RDY

IDE Ready. This is the input pin from the IDE Channel. It indicates that the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions.

See the references for details.

PIDE_IOR#/ SIDE_IOR#

IDE IOR# Command. This is the IOR# command output pin used to tell the IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.

PIDE_IOW#/ SIDE_IOW#

IDE IOW# Command. This is the IOW# command output pin used to notify the IDE device that the available Write Data is already asserted by the IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.

PIDE_INTRQ/ SIDE_INTRQ

Interrupt request signal from the IDE device.

HDRST#

Low-active hardware reset (RSTDRV inverted).

DASP_S

Time-multiplexed, open collector output that indicates that a drive is active. Also used for Master/Slave negotiation on the Secondary IDE channel.

As No IDE device, such as a Flash Disk, exists onboard the ETX module, this signal does not need to be connected to the DASP_S pin of any other device connected to the Secondary IDE channel.

PDIAG_S

The signal is used for Master/Slave negotiation on the Secondary IDE channel. It is asserted by the Slave to indicate to a master that the slave has passed its internal Diagnostic command.

As No IDE device, such as a Flash Disk, exists onboard the ETX module, this signal does not need to be connected to the DASP_S pin of any other device connected to the Secondary IDE channel.

On ETX modules that support DMA66 or DMA100, this pin may additionally be used to detect the presence of the 80 conductor IDE cable which is required to support these modes.

CBLID_P#

On ETX modules that support DMA66 or DMA100, this pin may be used to detect the presence of an 80 conductor IDE cable on the primary IDE channel. This allows BIOS or system software to determine whether to enable high-speed transfer modes.

9.4.2 Ethernet Signals

The ETX Ethernet Interface is designed for use with an external 1:1/ 1:1 transformer.

TXD#, TXD (ANALOG TWISTED PAIR)

Ethernet Transmit Differential Pair. These pins transmit the serial bit stream on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.

RXD#, RXD (ANALOG TWISTED PAIR)

Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. The bit stream can be transmitted in either two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.

ACTLED

The Activity LED pin indicates either transmitted or received data activity on the Ethernet port. This pin is asserted low when activity is detected. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

LILED

The Link Integrity LED pin indicates link integrity. This pin is asserted low when the link is valid. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

SPEEDLED

The Speed LED pin indicates high speed operation. This LED is not supported by all ETX boards. This pin is asserted low when a 100Mbps link is detected, and is not asserted for a 10Mbps link. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

9.4.3 Power control signals

PWGIN

An active-high input to the ETX from an external power supply, indicating that the power is good and that the ETX can begin booting. Usage of this signal is not required because the ETX module contains its own power-good logic.

The PWGIN signal can be used as an active-low reset input to the ETX module. Leave as a no-connect if reset function not required.

5V_SB

Power input for the internal suspend and power control circuitry. Connect to a 5V, 100mA stand-by power source. Leave as a no-connect if a standby power supply is not available.

PS_ON

Active-low output from ETX module. This can be connected to the PS_ON input of an ATX power supply in order to switch the main output. In order for this pin to function, 5V_SB must be supplied to the ETX module.

PWRBTN#

Power Button Input. Connect to GND with momentary-contact switch or open collector driver to implement ATX power button control of PS_ON. In order for this pin to function, 5V_SB must be supplied to the ETX module.

9.4.4 Power management signals

RSMRST#

Resume Reset input. This input may be driven low by external circuitry in order to reset the power management logic on the ETX module.

SMBALRT#

Not implemented

BATLOW#

Not implemented

GPE1#

Not implemented

GPE2#

Not implemented

EXTSMI

Not implemented

9.4.5 Miscellaneous Signals

SPEAKER

PC speaker output signal. This logic-level signal can be connected to an external transistor in order to drive a piezoelectric or dynamic speaker.

BATT

3V backup cell input. BATT can be connected to a 3V lithium backup cell for RTC operation and CMOS register non-volatility in the absence of system power.

I 2 CLK, I 2 DAT

Not implemented

SMBDATA, SMBCLK

System Management Bus clock and data lines. These lines may be used to support external devices such as temperature and battery monitoring chips.

SMBUS address 00 is used by the presence detect EEPROM on the DDR RAM module.

KBINH

Keyboard Inhibit. Not supported.

OVCR#

Over-current detect input. Used to monitor the USB power over-current. Pull with open collector to GND if over-current is detected.

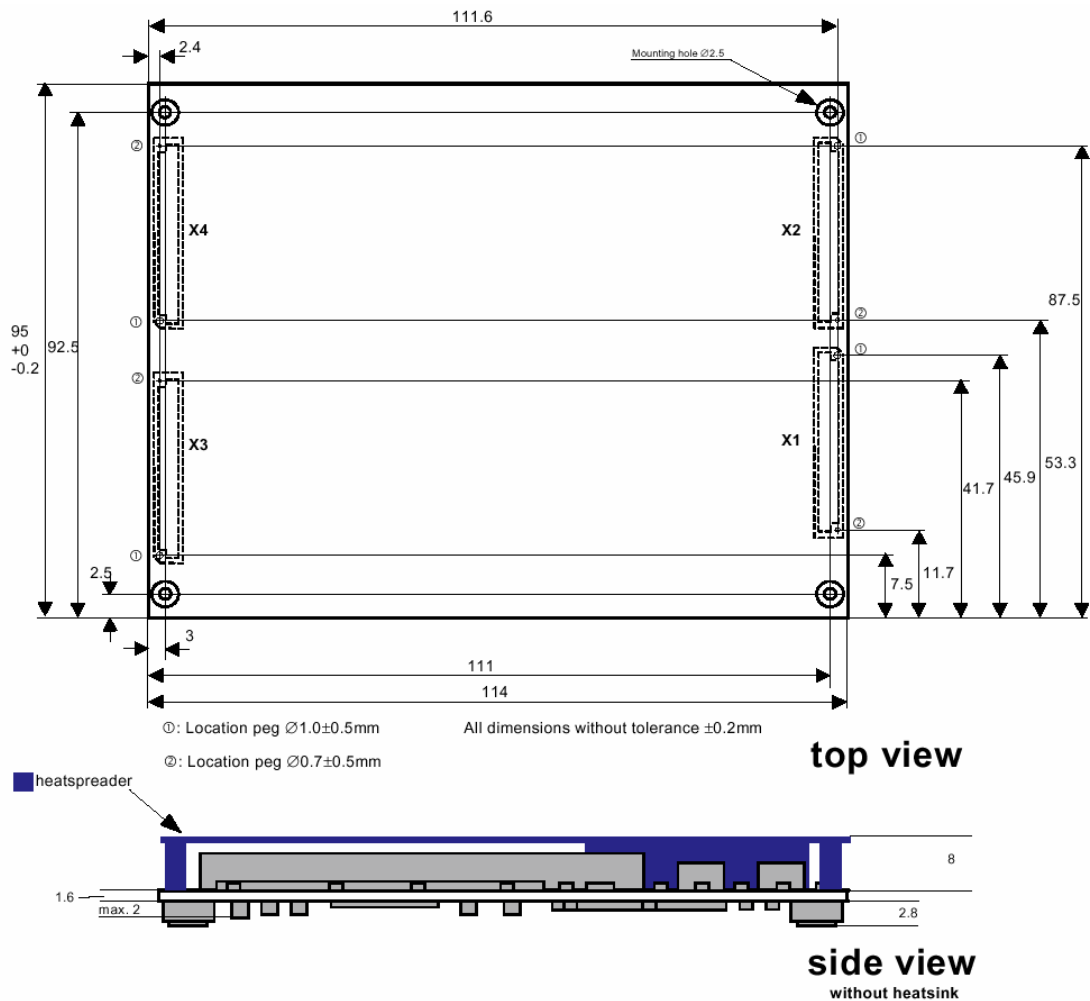
ROMKBCS#, EXT_PRG

Reserved. Do not connect to this pin.

GPCS#

Reserved. Do not connect to this pin.

10 PCB DIMENSIONS AND FIXING POSITIONS.



Note: The GX533 ETX module does not require a heat spreader or heatsink when used in an ambient temperature range up to 55 degrees C. For extended temperature range operation please contact DSL.